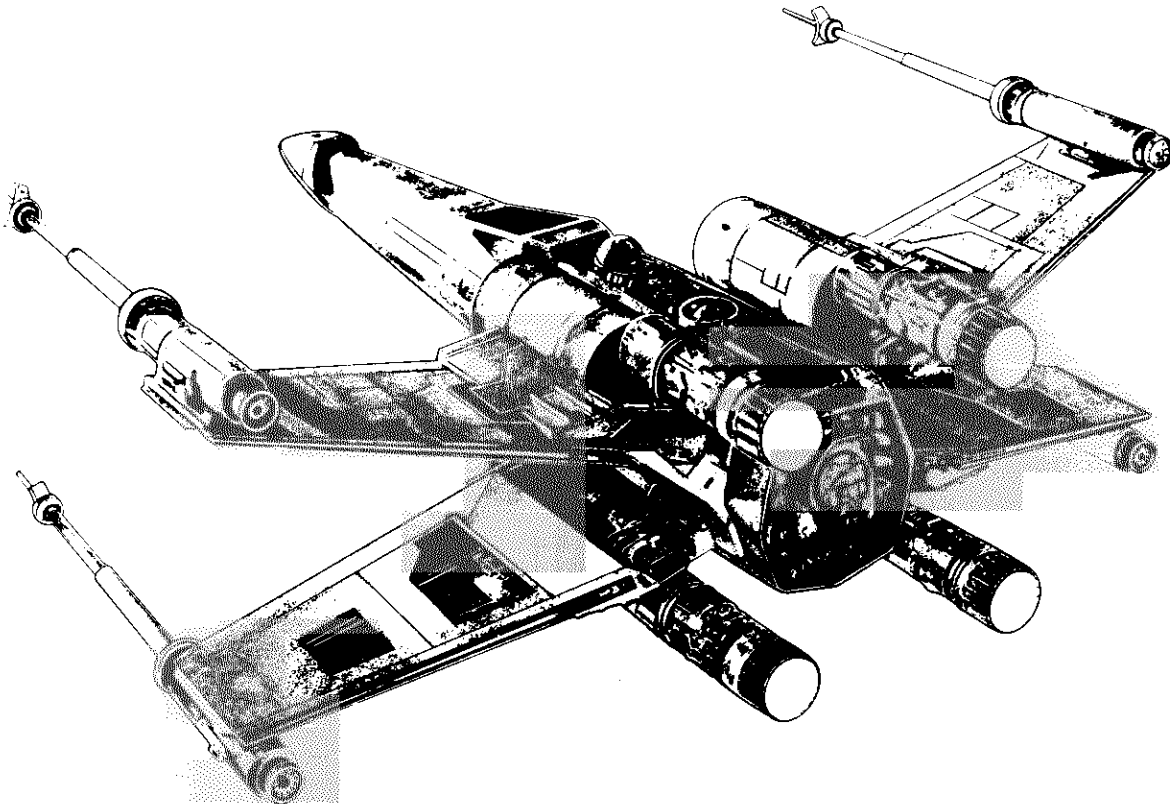


NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.



www.atari-history.com

Schematic Package Supplement to

STAR WARS*

Operators Manual

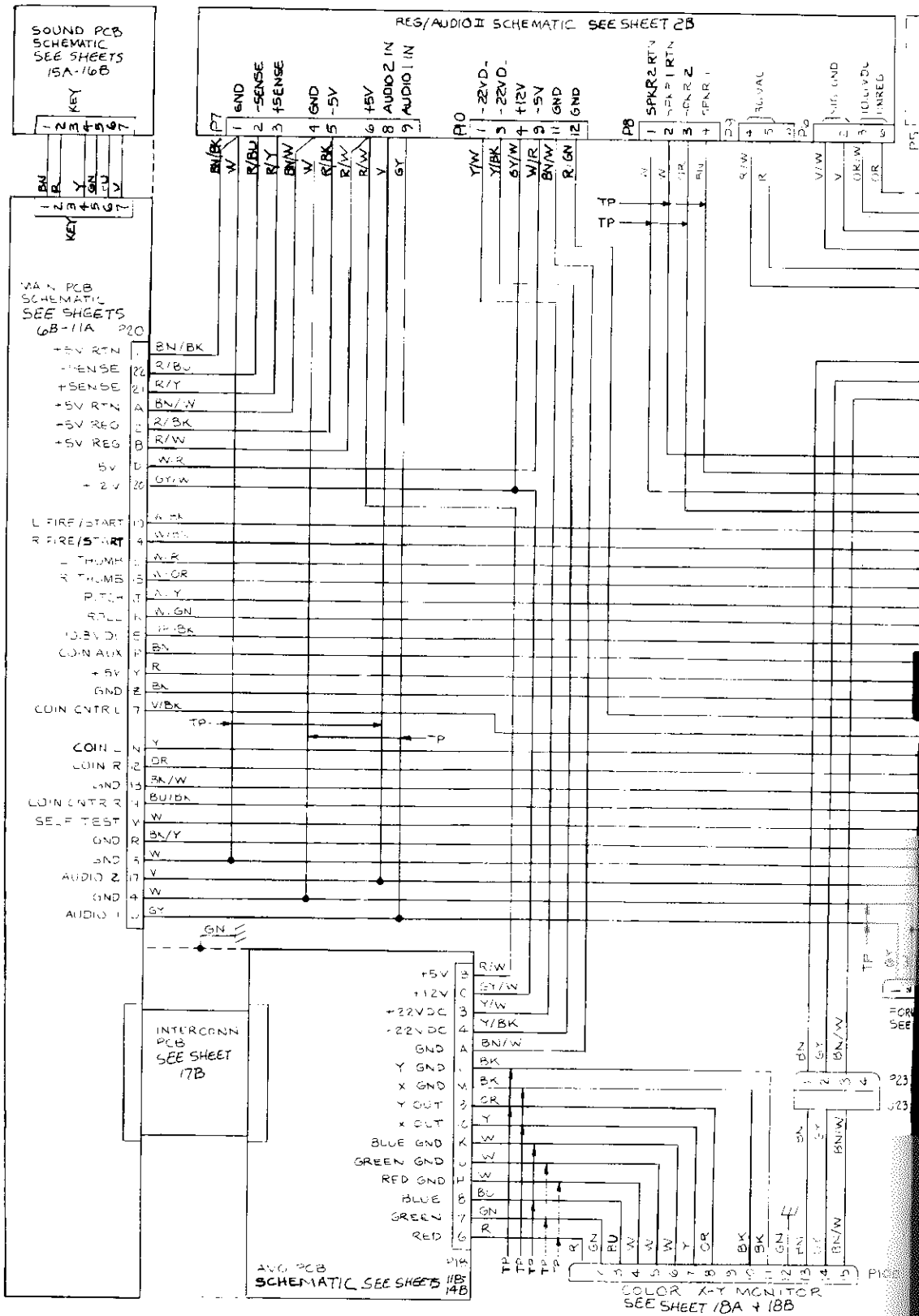
*Trademarks of Lucasfilm, Ltd. used by Atari, Inc. under license.

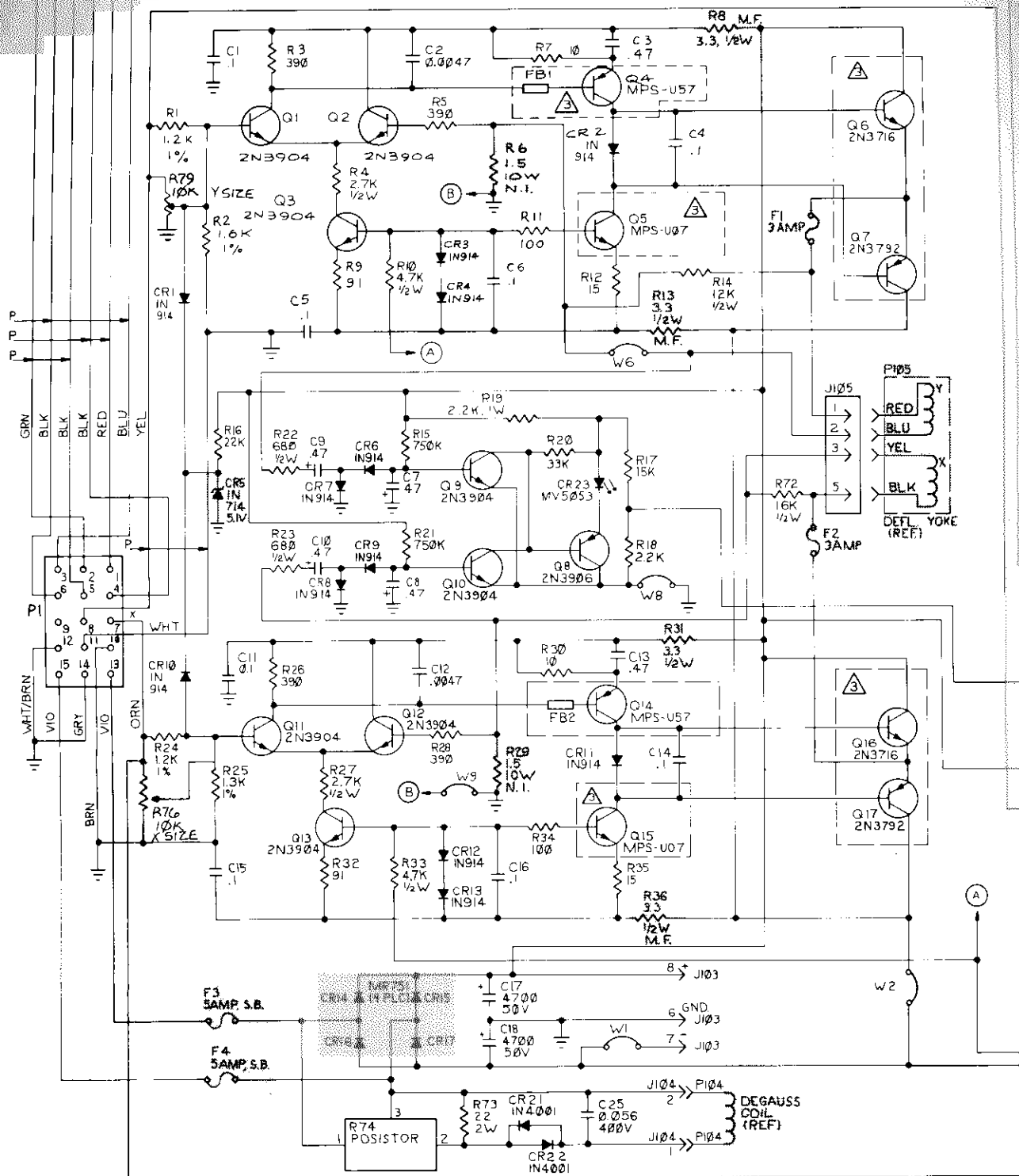
6M



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SP-225 Sheet 1A
1st printing





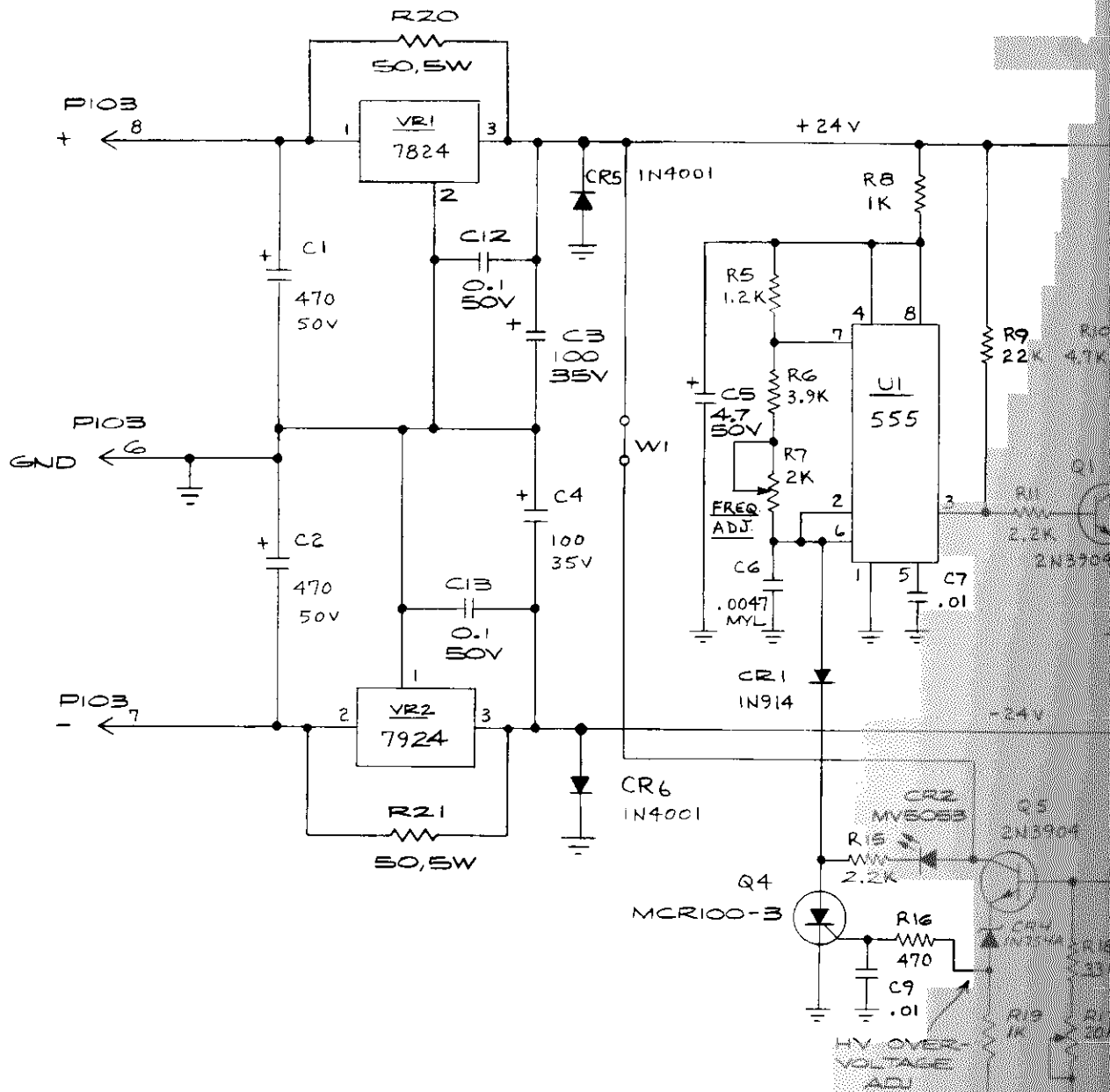


1. ALL RESISTOR VALUES IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE μf .

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SP-225 Sheet 18A
1st printing



P3

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STAR WARS Interconnect PCB

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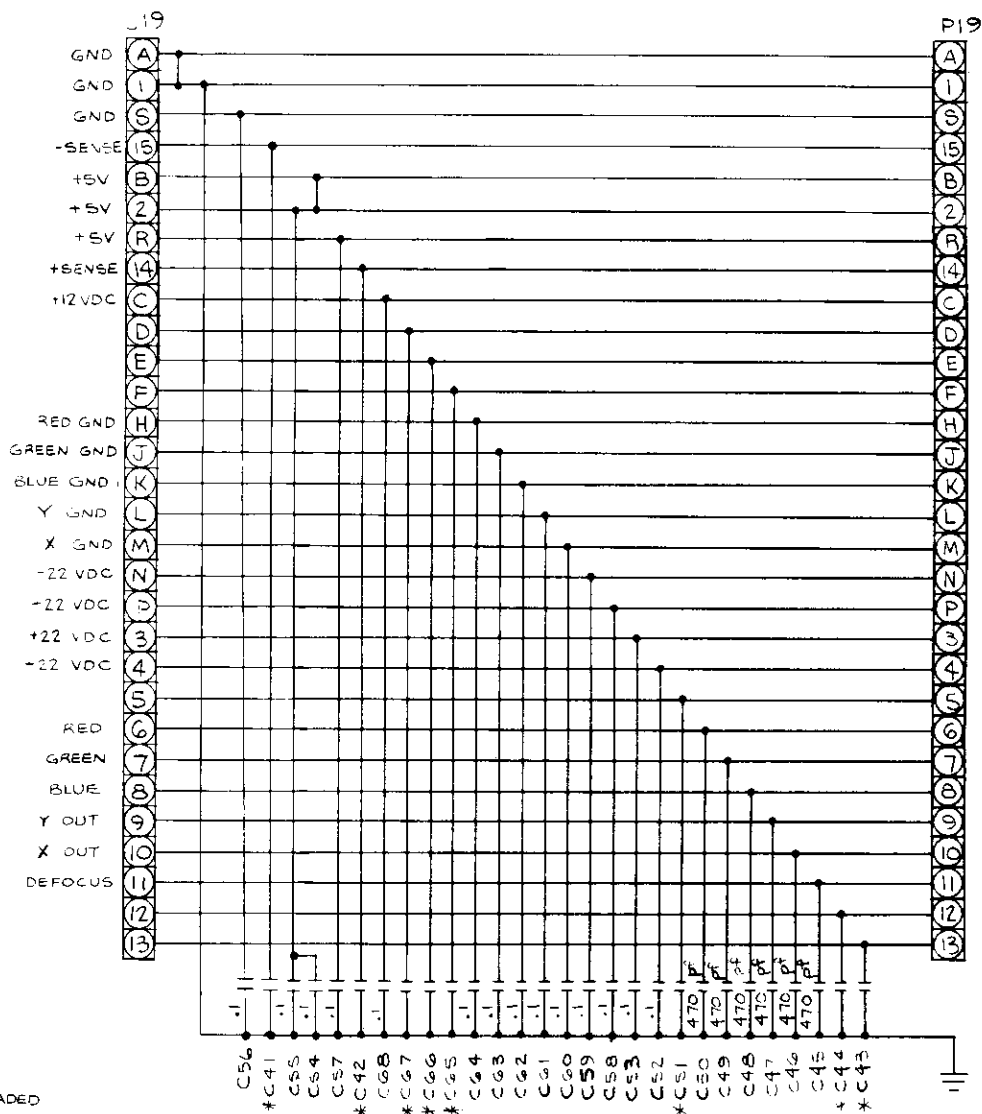
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SP-225 Sheet 17B
1st printing

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J20

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NOTE:

1. * = NOT LOADED

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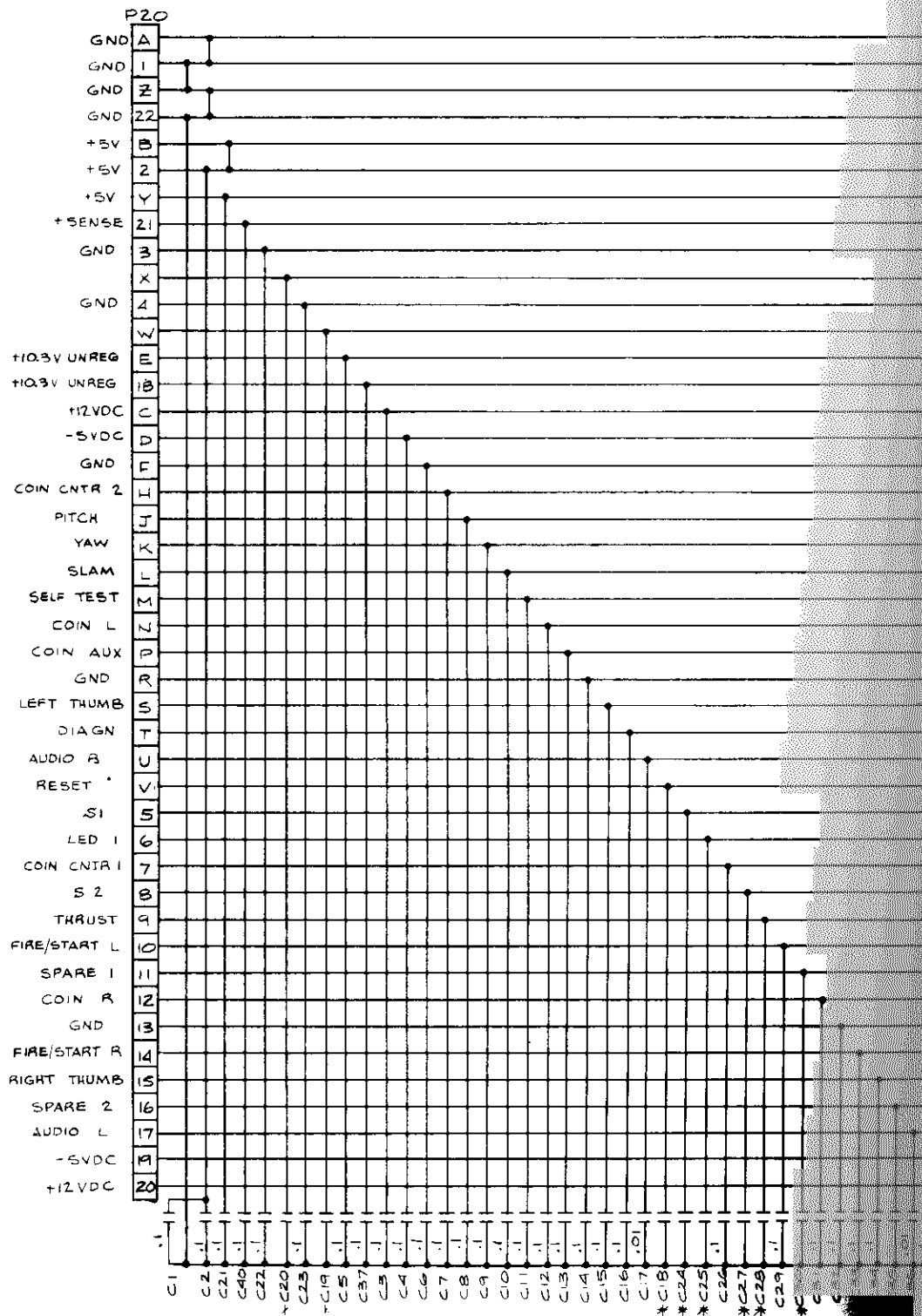
STAR WARS EMI Shield PCB



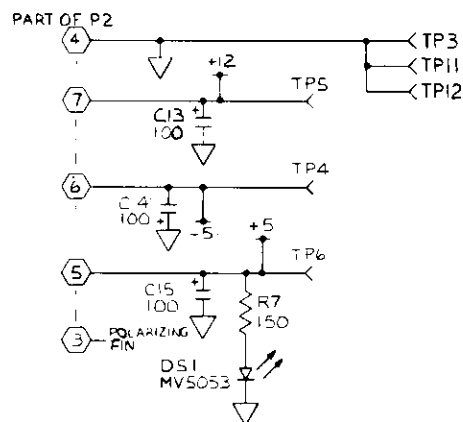
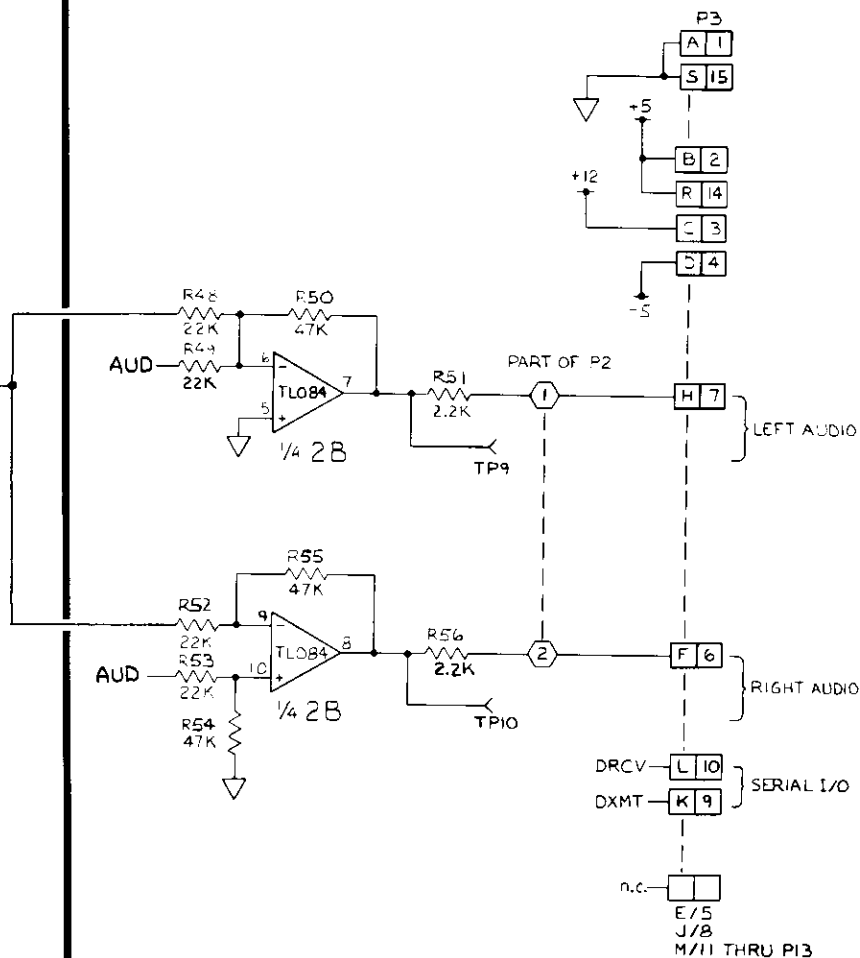
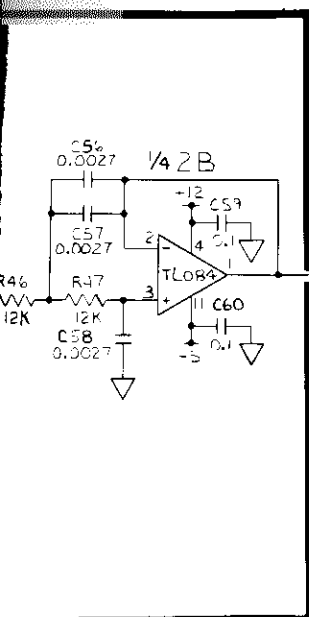
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Output and Summing Amplifiers



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STAR WARS Sound PCB

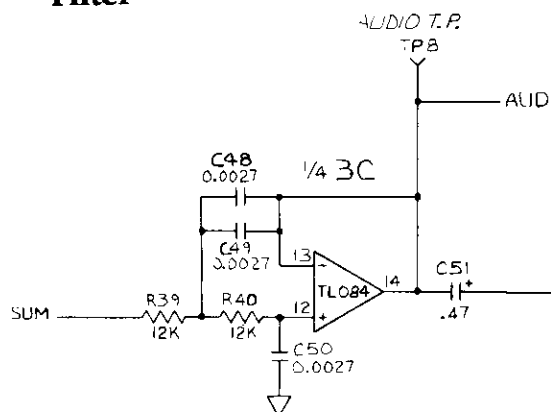


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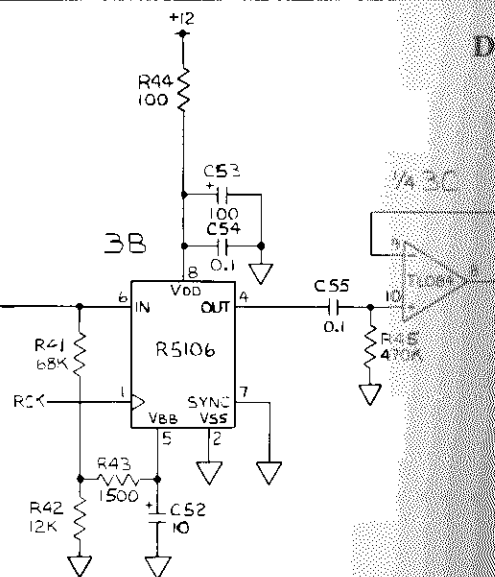
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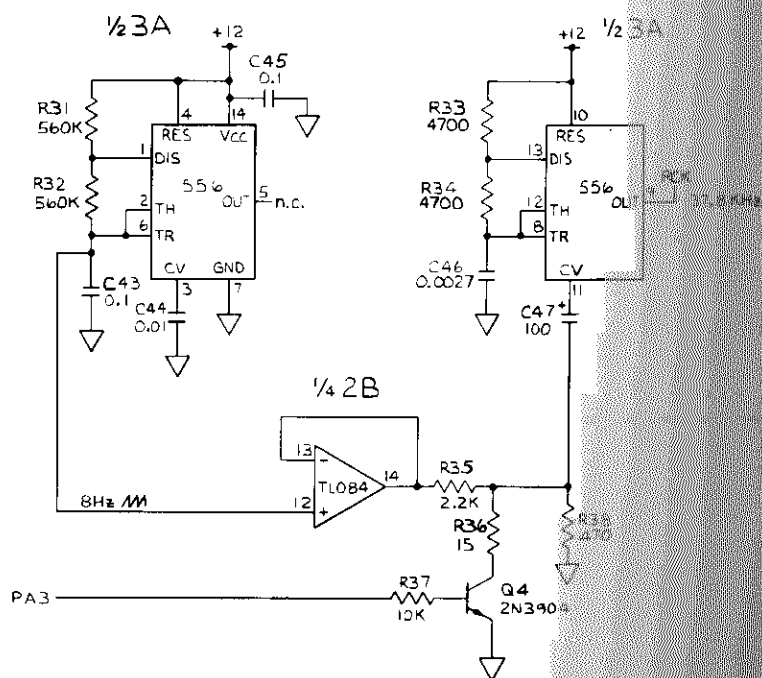
Filter

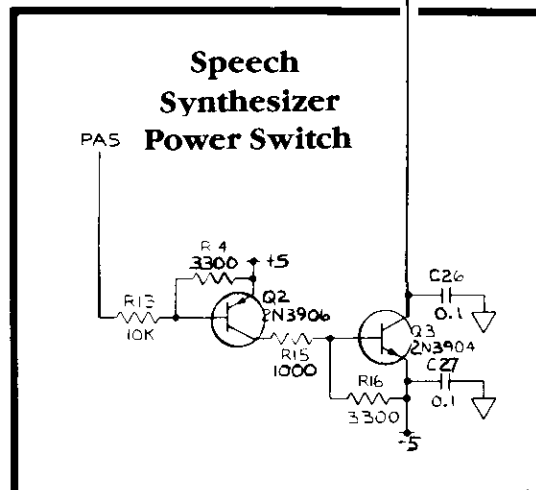
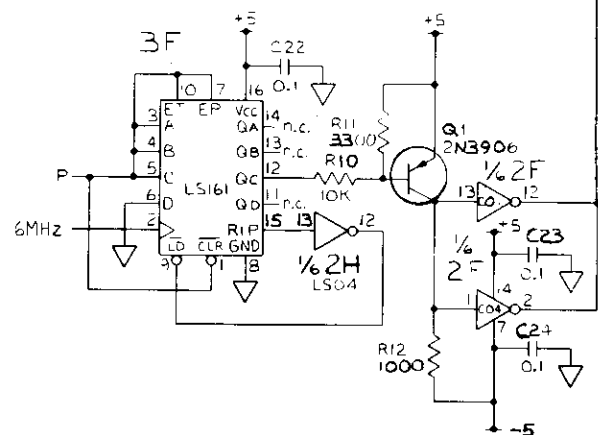
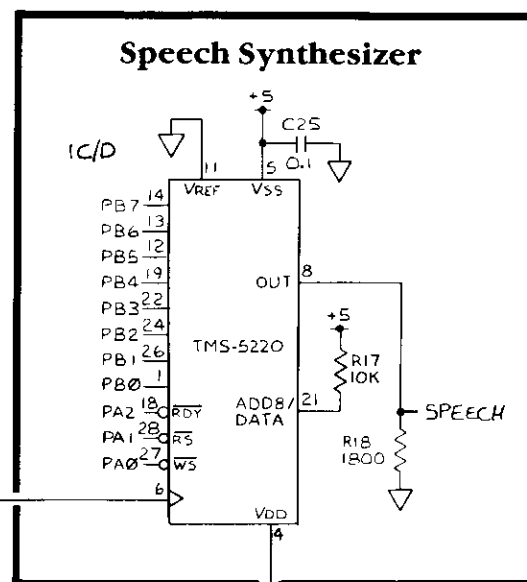
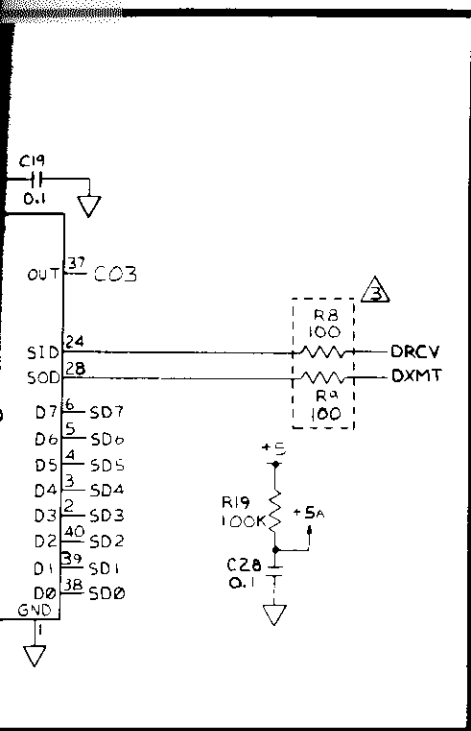


Delay



Delay Clock





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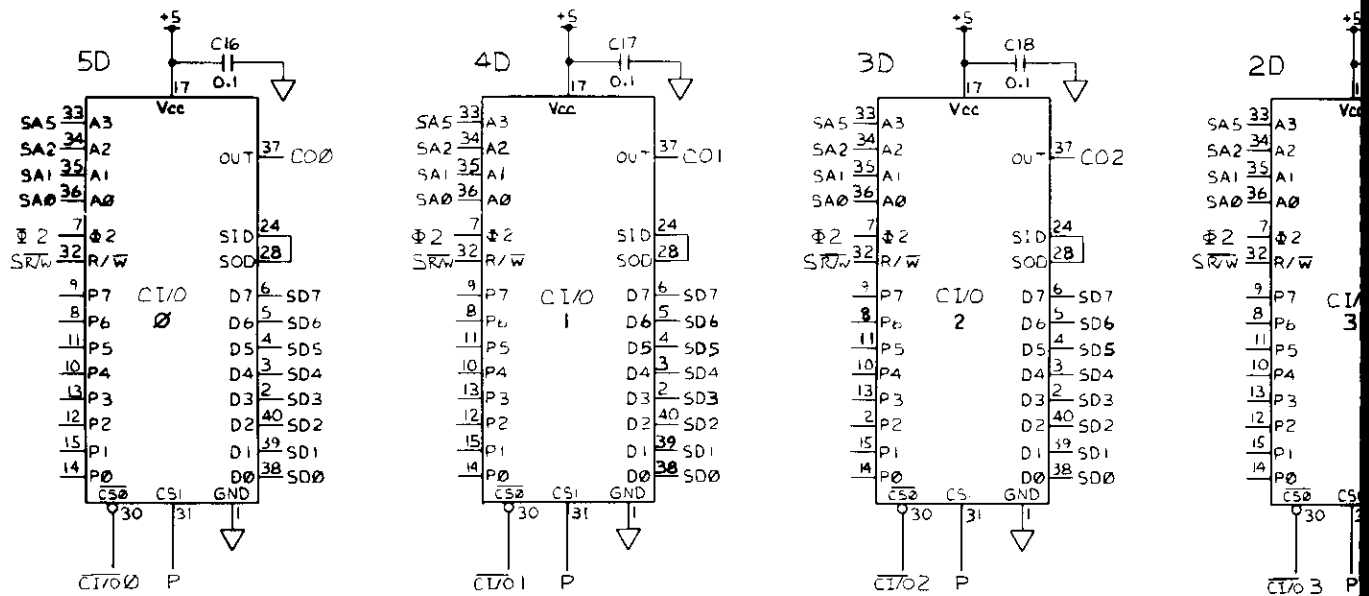


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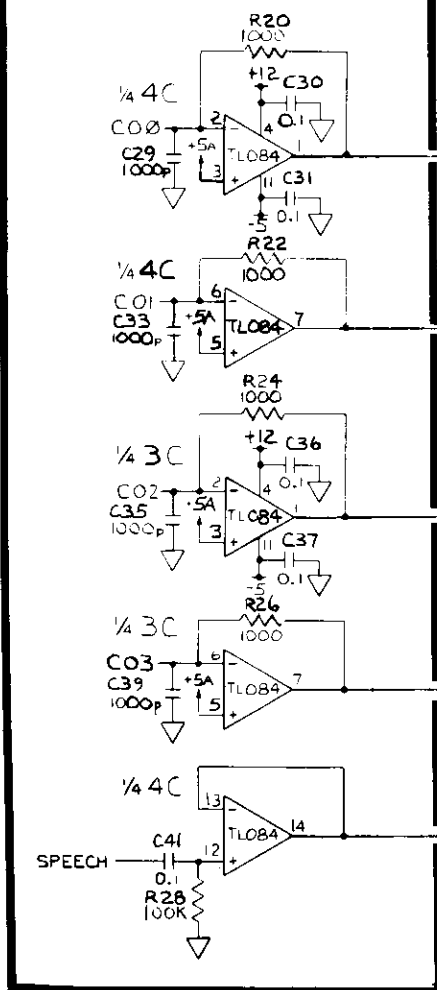
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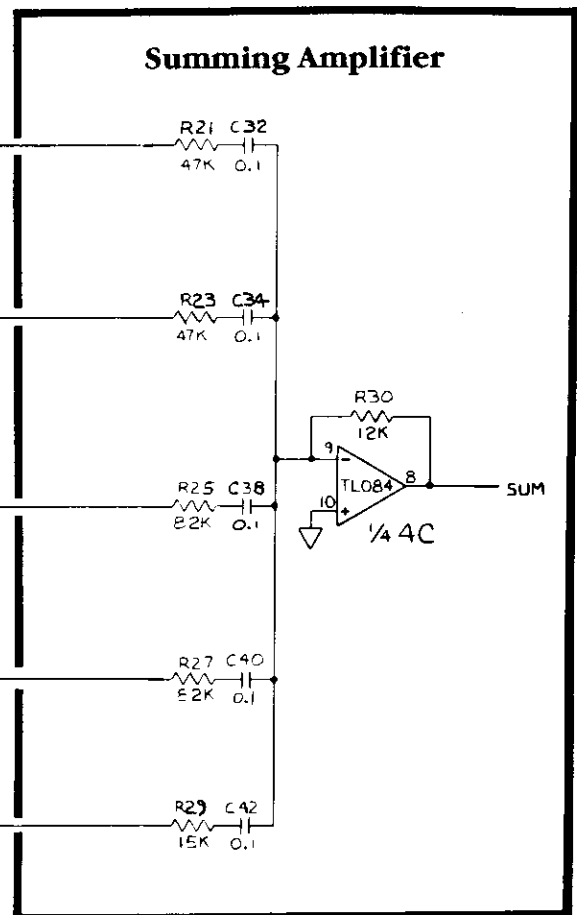
Music and Sound Effects Generators

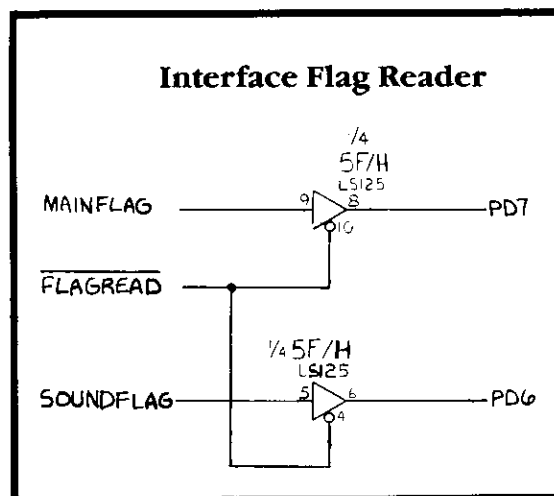
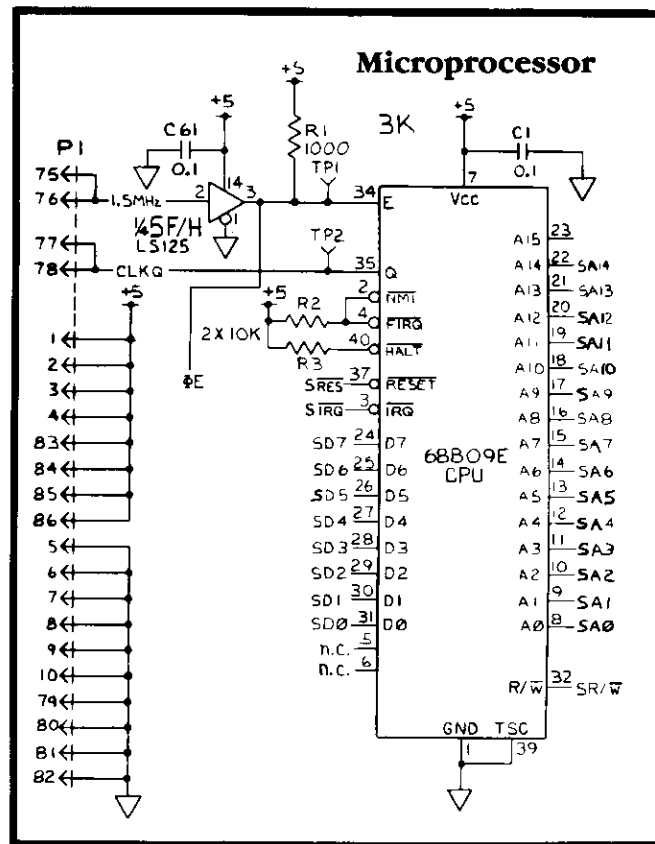
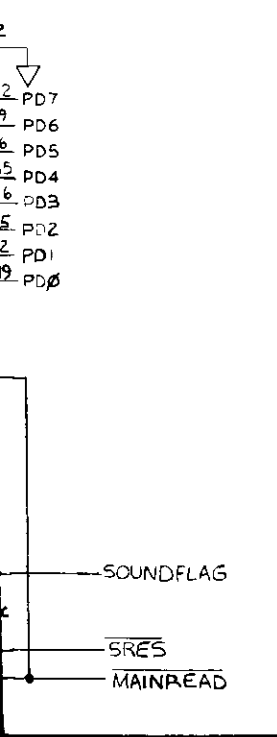
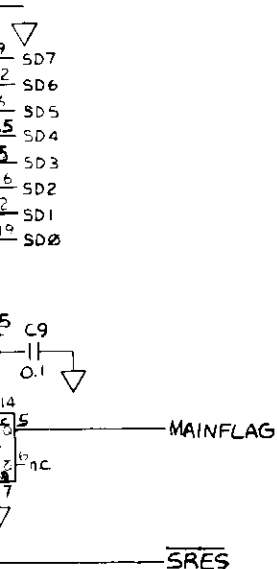


Buffers



Summing Amplifier





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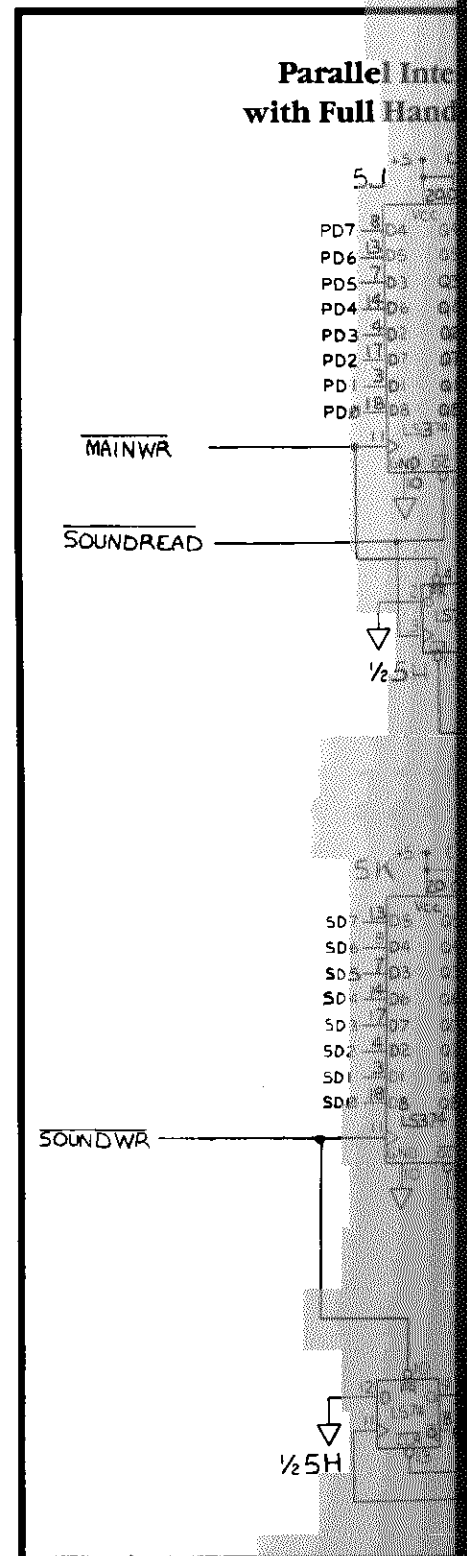
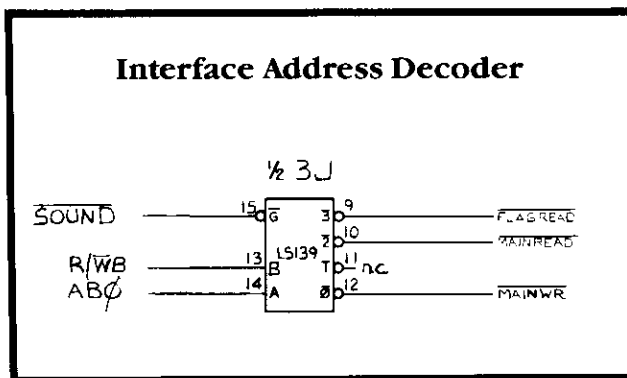
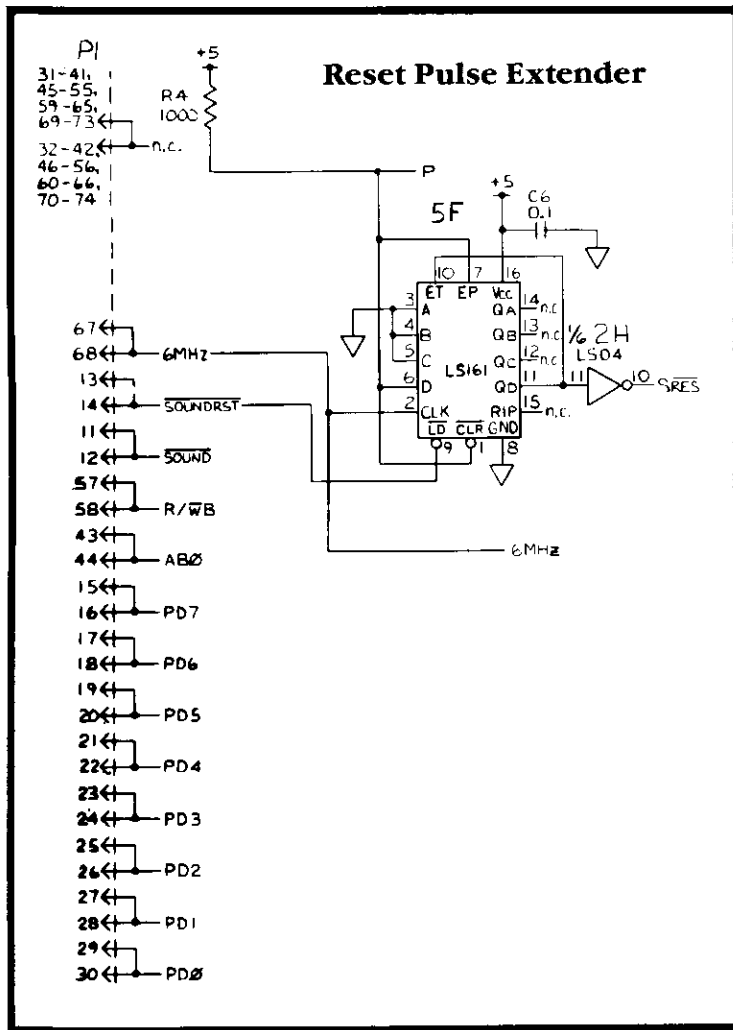
STAR WARS Sound PCB



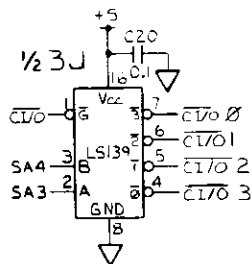
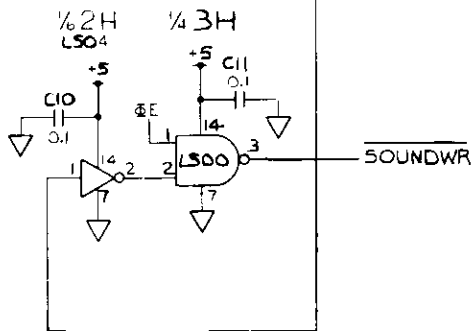
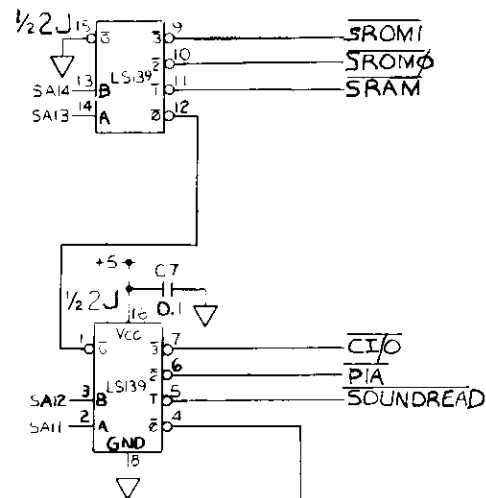
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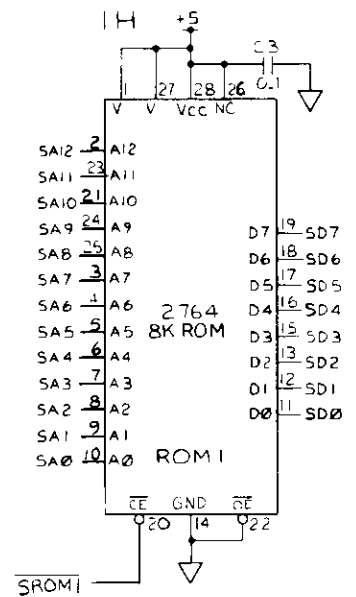
SP-225 Sheet 15A
1st printing



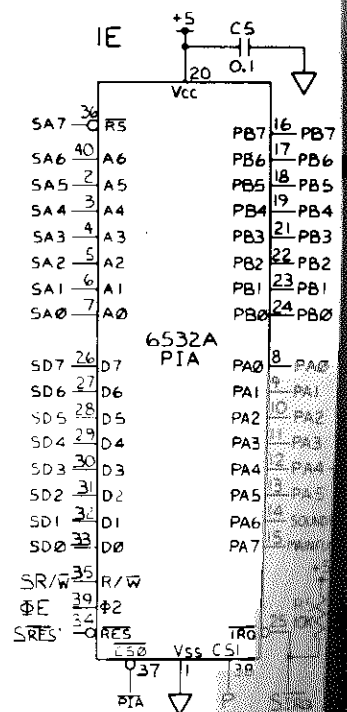
Address Decoders



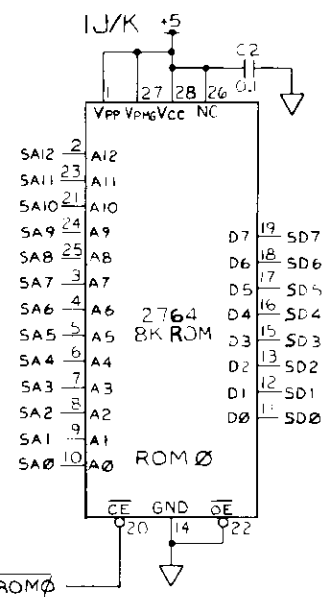
Sound



Peripheral Inter



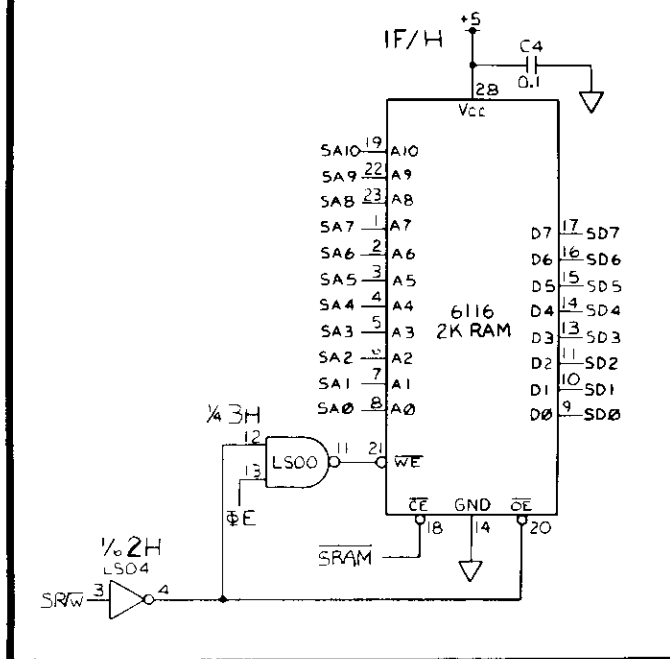
ROM



ice Adapter



Sound RAM



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STAR WARS Sound PCB



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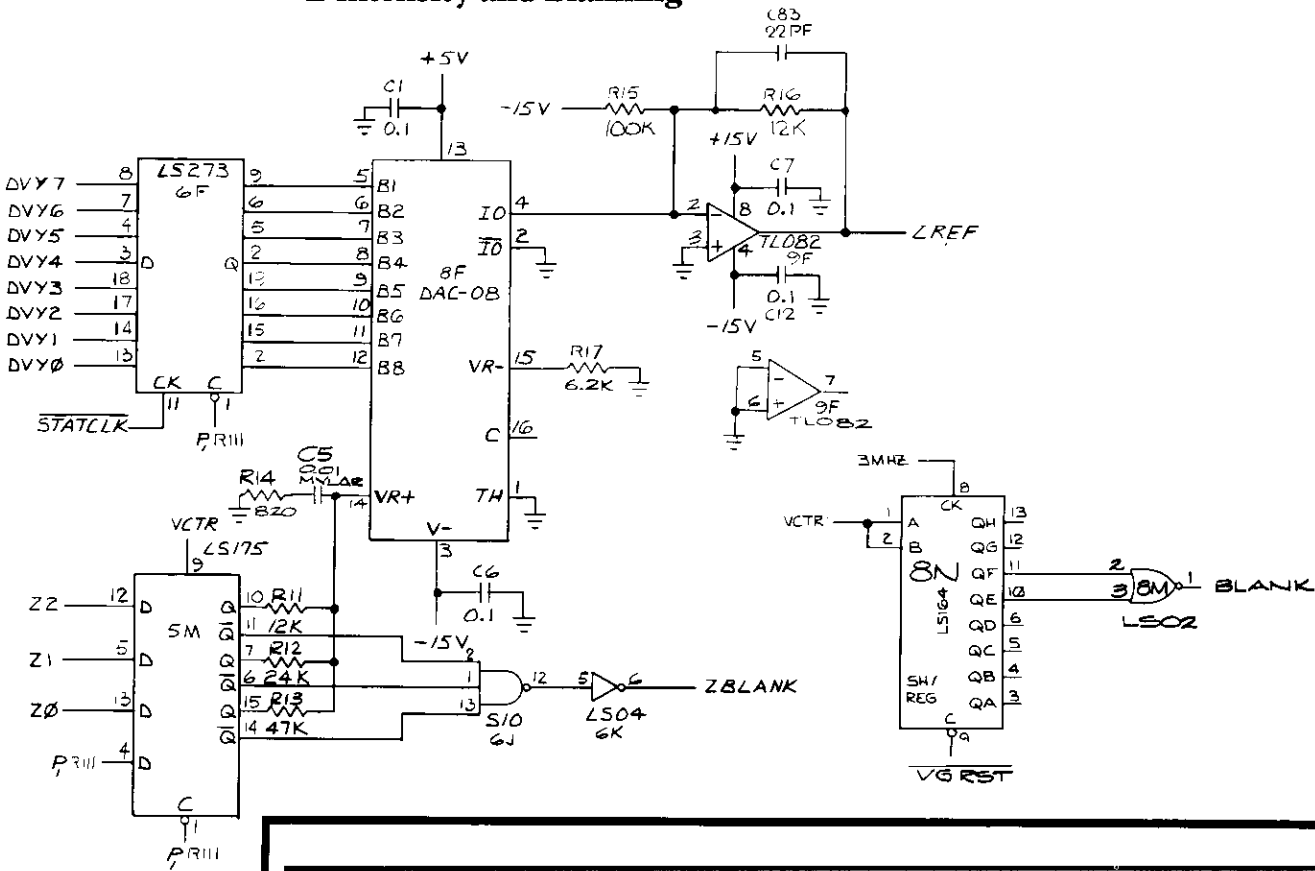
SP-225 Sheet 15B
1st printing

Bipolar Offset Adjustments

Perform the following procedure to adjust the bipolar offset current:

1. Set the game to the Self-Test Mode and select the Bipolar Offset Test Display as described in Chapter 2 of the game manual.
2. Adjust XBIP (R92) and YBIP (R88) so that the displayed-box line width is $\frac{1}{8}$ -inch or less.

Z-Intensity and Blanking



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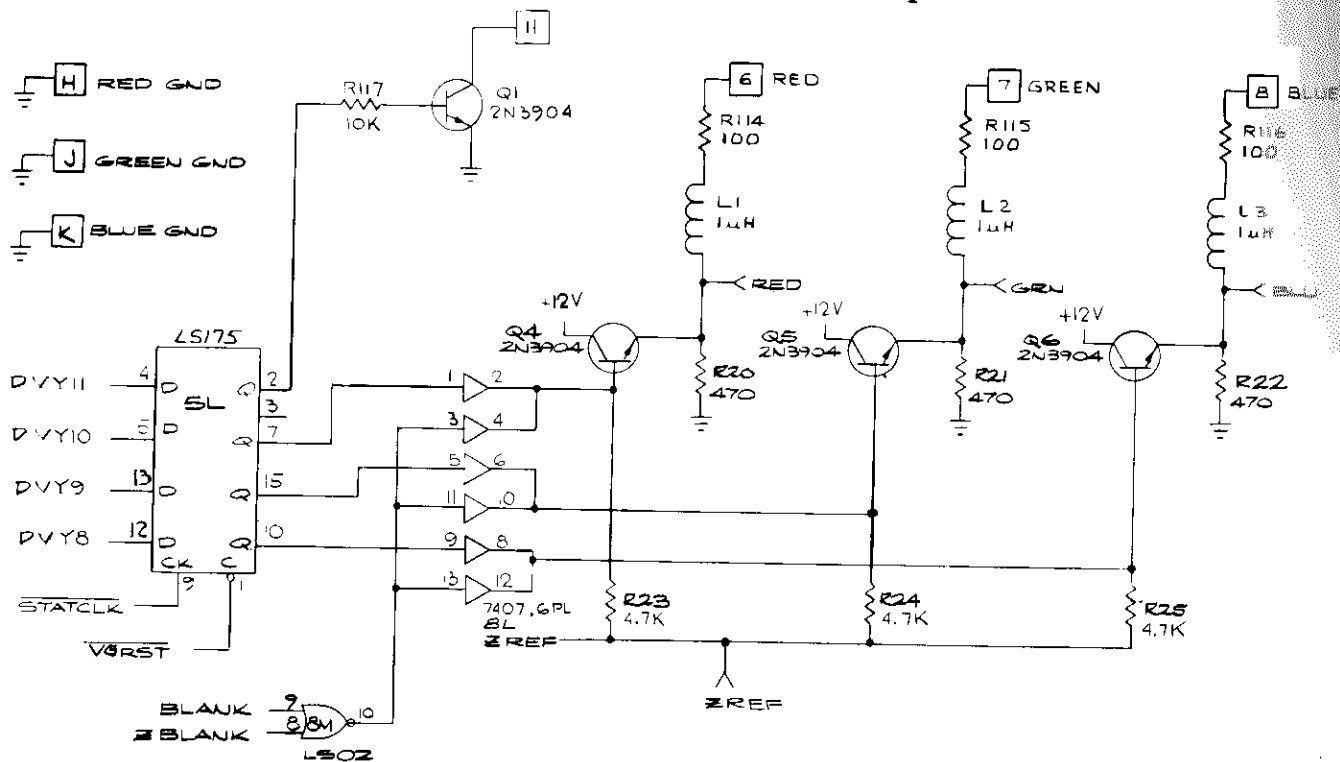
STAR WARS Analog Vector-Generator PCB

 A Warner Communications Company

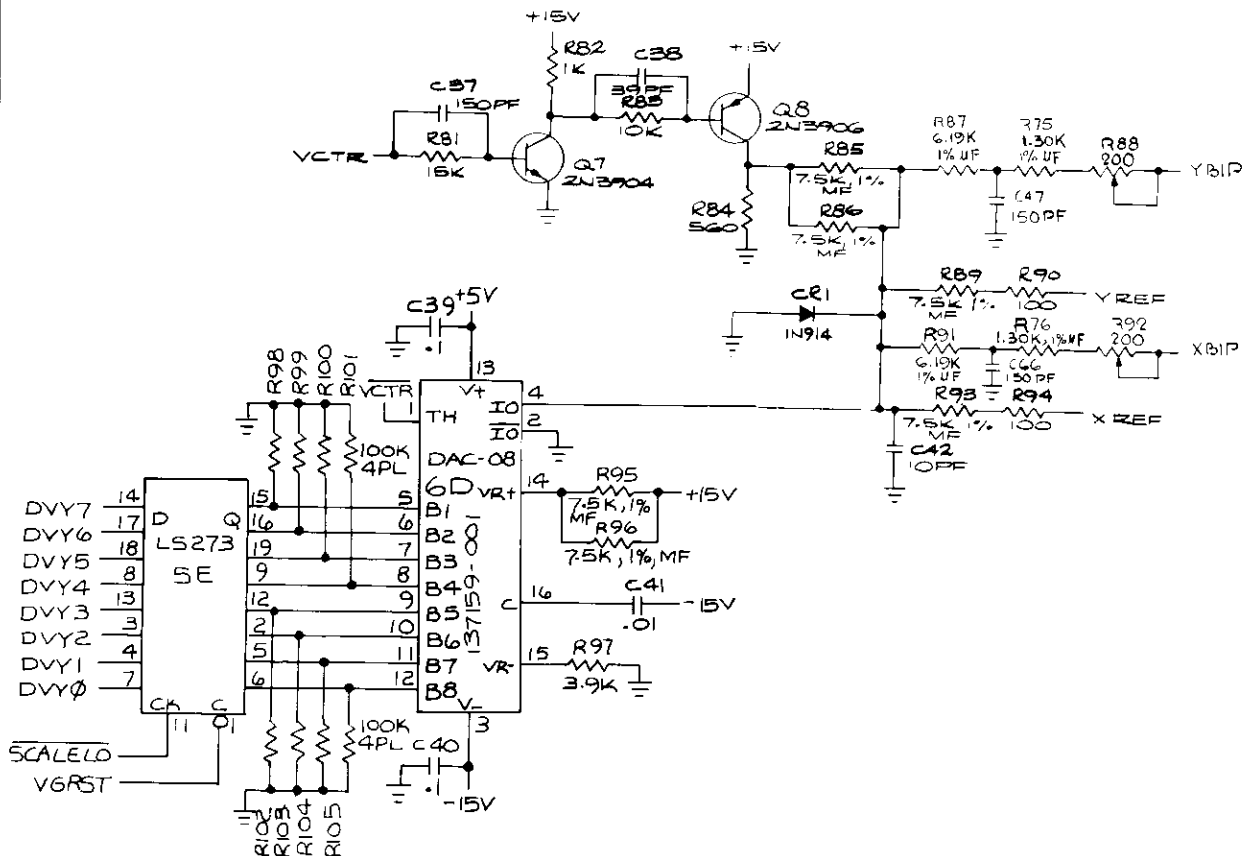
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SP-225 Sheet 14B
1st printing

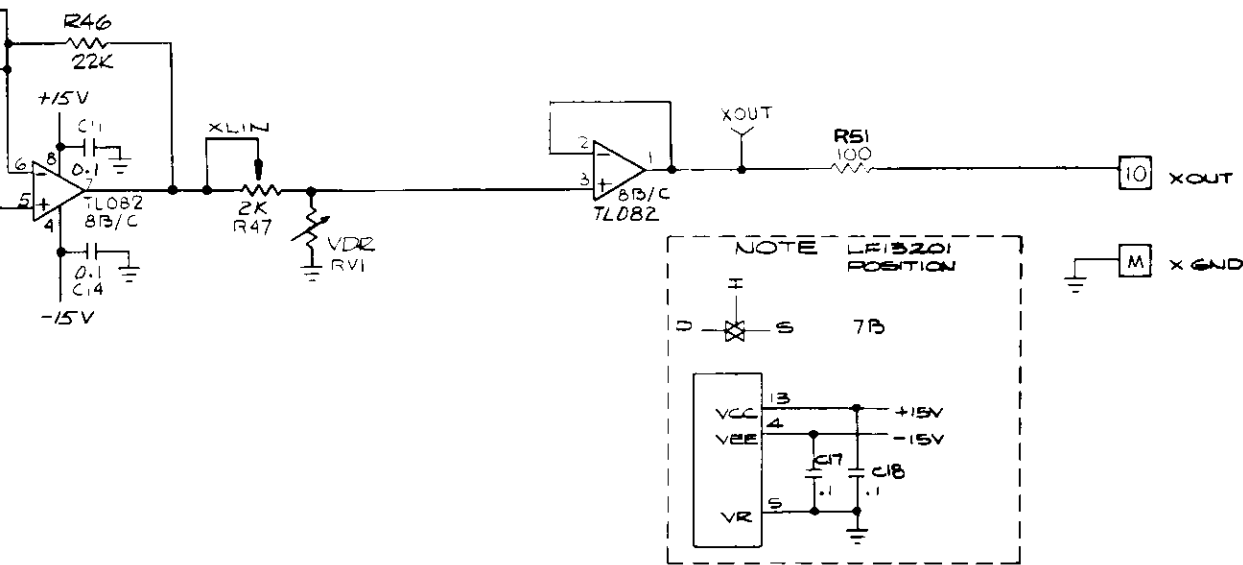
R-G-B Output



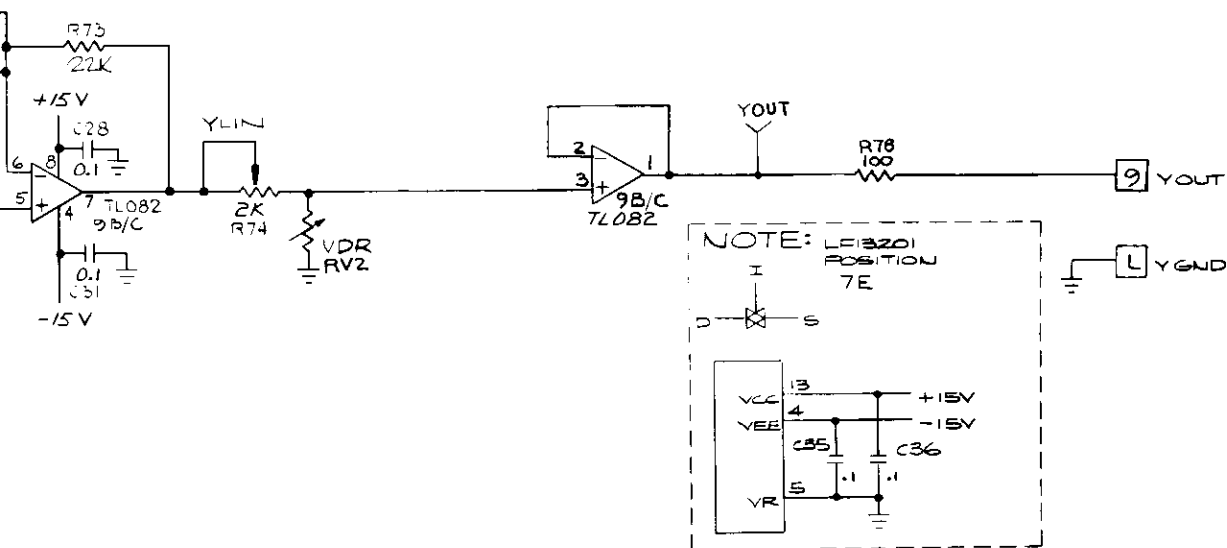
DAC Reference and Bipolar Current Sources



X-Axis Output



Y-Axis Output



that the cross-
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play.

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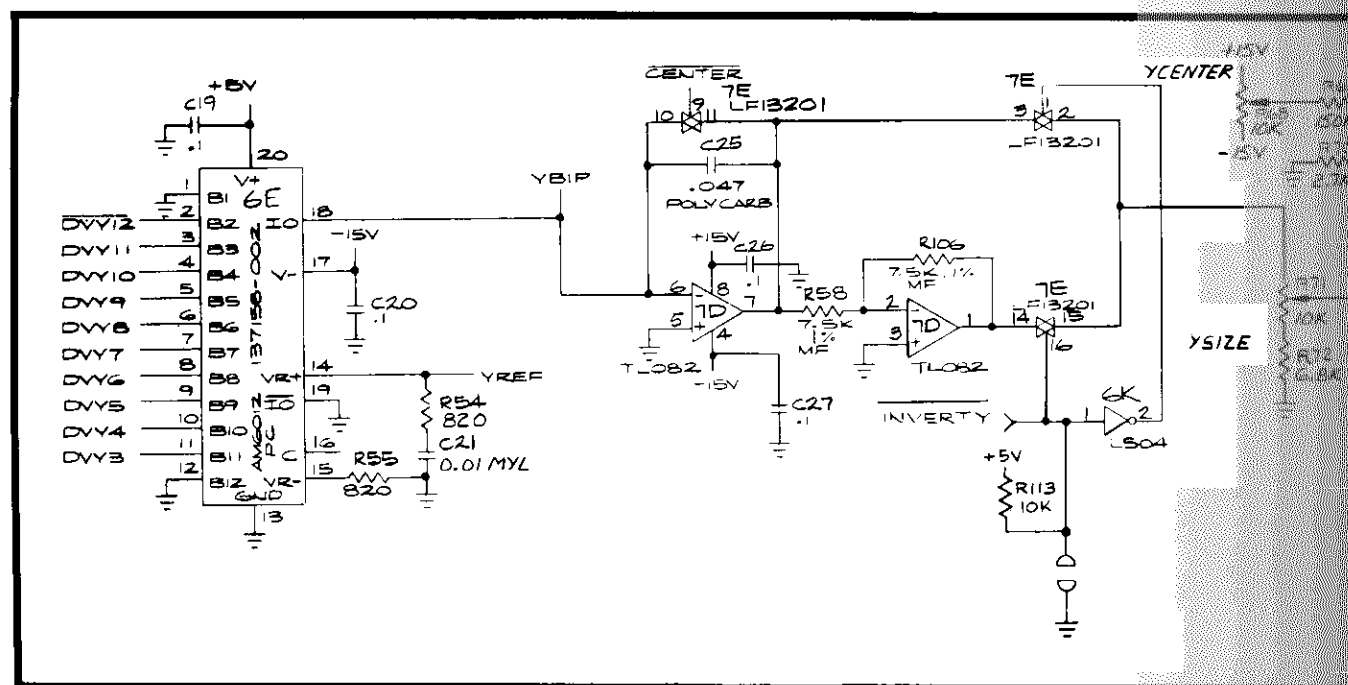
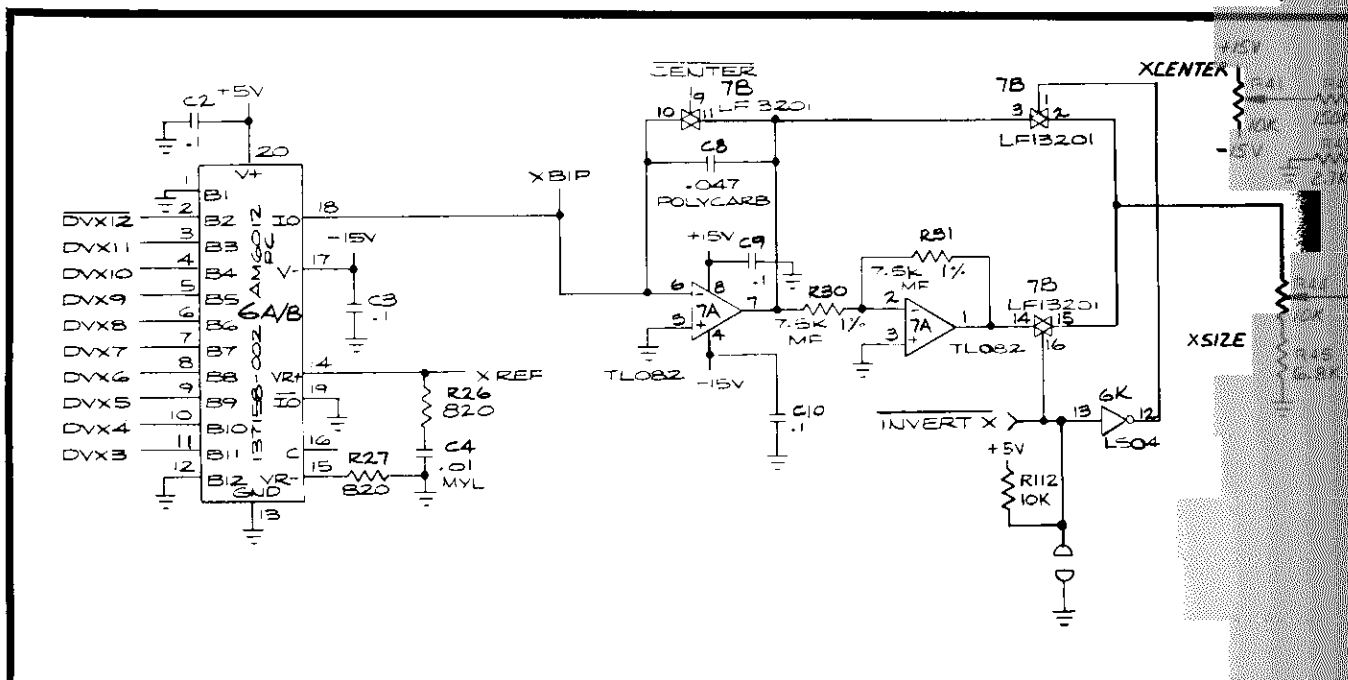
STAR WARS Analog Vector-Generator PCB



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1st printing



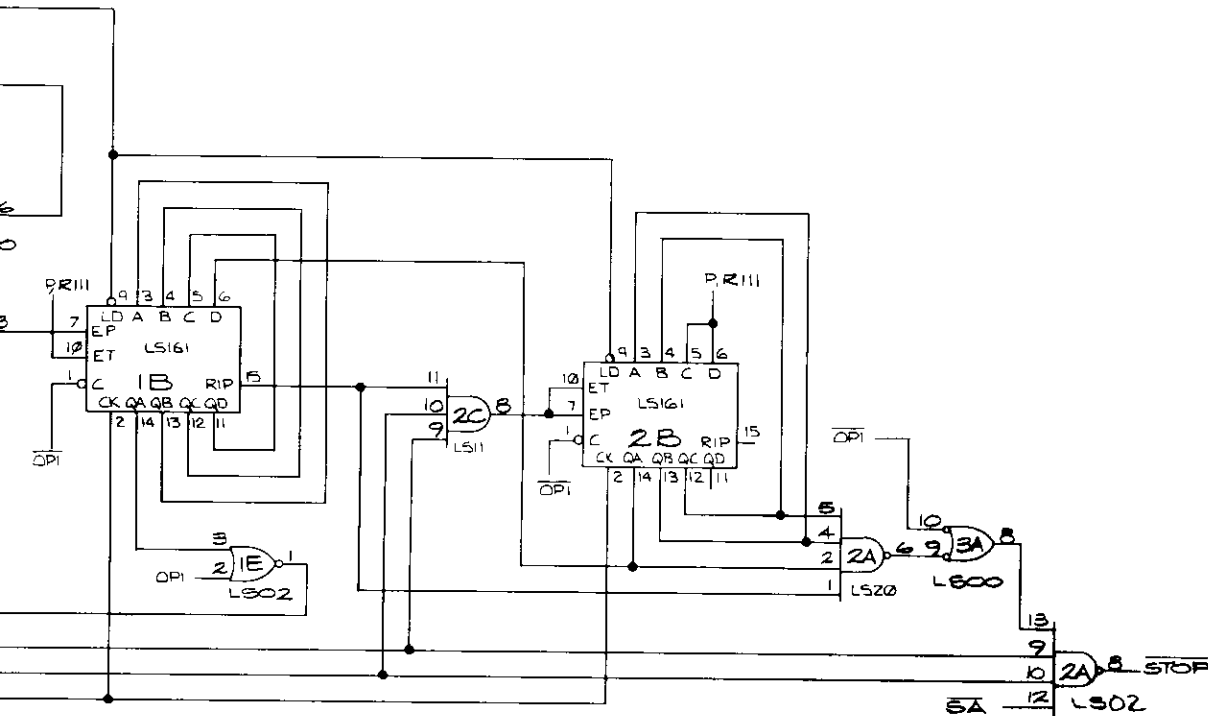
X and Y Video Adjustments

Perform the following procedure to adjust the display size, centering, and linearity:

1. Set the game to the SelfTest Mode and select the Cross-hatch Pattern Display as described in Chapter 2 of the game manual.
2. Adjust XCENTER (R41) and YCENTER (R68) so that the crosshatch pattern is centered on the screen.

3. Adjust XSIZE (R44) and YSIZE (R71) so that the hatch pattern covers the entire visible area of the screen.
4. Adjust XLIN (R47) and YLIN (R74) so that the lines are straight and the diamond shape is symmetrical. Since the linearity adjustment changes the size of the display, it may be necessary to repeat step 3 to obtain the correct display size.

Vector Timer



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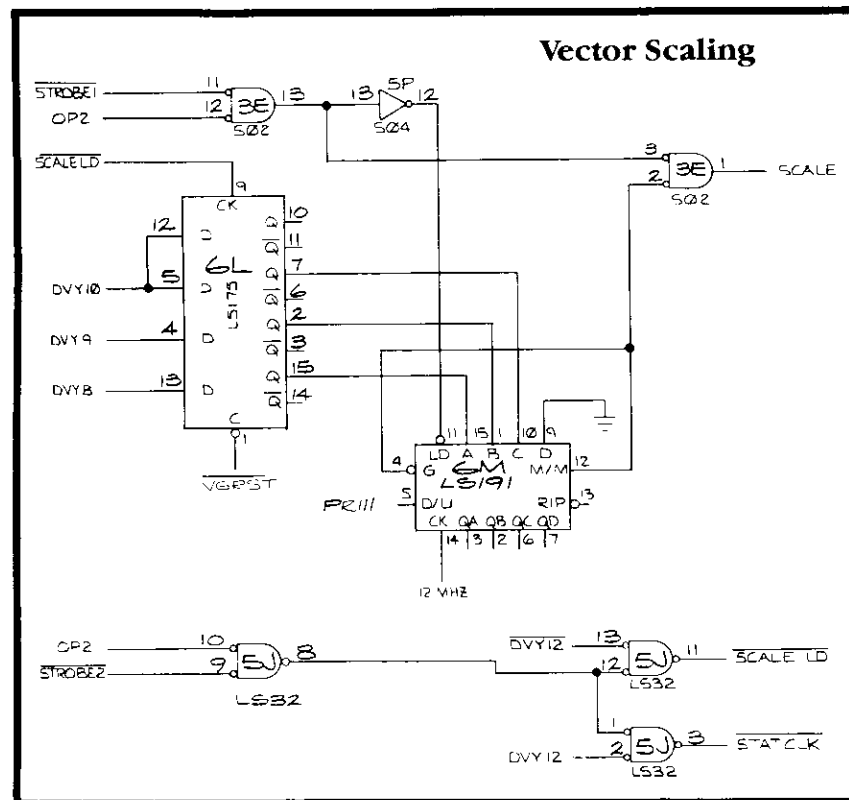
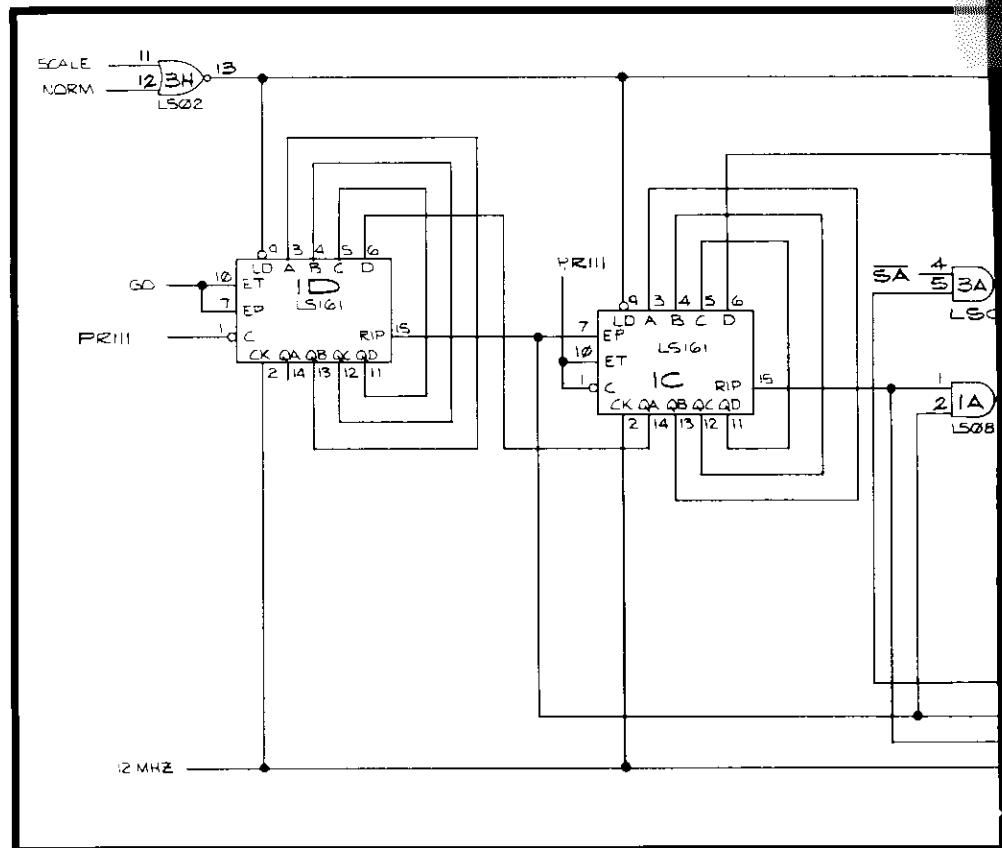
STAR WARS Analog Vector-Generator PCB



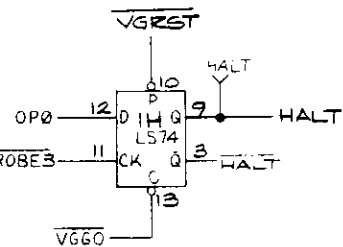
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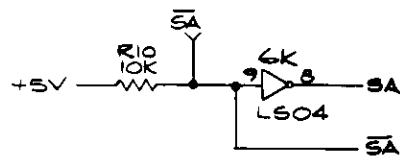
SP-225 Sheet 13B
1st printing



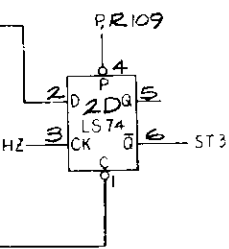
Halt Flag



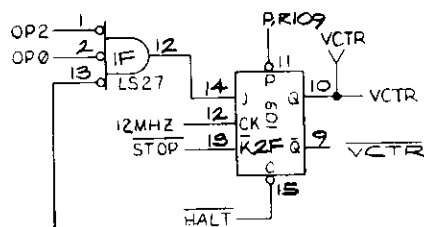
Signature Analysis



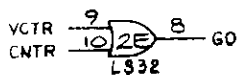
der Disable



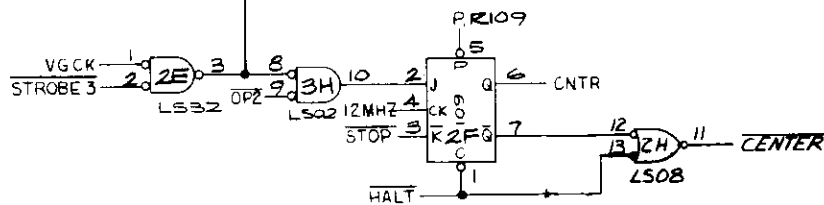
Vector Flag



Go Flag



Center Flag



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STAR WARS Analog Vector-Generator PCB



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Vector Address Decoder

The diagram illustrates a Vector Address Decoder circuit. It features a 2K 1542 decoder chip with inputs A, B, C, and D, and outputs 0 through 9. The inputs are connected as follows:

- Input D is connected to a ground symbol.
- Input C is connected to AMI13.
- Input B is connected to AMI12.
- Input A is connected to AMI11.

The outputs of the decoder are connected to various components:

- Output 0 is connected to VRAM0.
- Output 1 is connected to VRAM1.
- Output 2 is connected to VRAM2.
- Output 3 is connected to VRAM3.
- Output 4 is connected to VRAM4.
- Output 5 is connected to VRAM5.
- Output 6 is connected to an AND gate (LS08) along with output 4. The output of the AND gate is connected to VRAM.
- Output 7 is connected to the AND gate (LS08) along with output 4. The output of the AND gate is connected to VRAM.
- Output 8 is connected to the AND gate (LS08) along with output 4. The output of the AND gate is connected to VRAM.
- Output 9 is connected to the AND gate (LS08) along with output 4. The output of the AND gate is connected to VRAM.

Vector ROM

Microprocessor Pin	Microprocessor Label	ROM Pin	ROM Label	External Signal
21	AM11	A11	D7	DV6 7
19	AM10	A10	D6	DV6 6
22	AM9	A9	D5	DV6 5
23	AM8	A8	D4	DV6 4
1	AM7	A7	D3	DV6 3
2	AM6	A6	D2	DV6 2
3	AM5	A5	D1	DV6 1
4	AM4	A4	D0	DV6 0
5	AM3	A3		
6	AM2	A2		
7	AM1	A1		
8	AM0	A0		

ROM: 2732

OE (pin 20) → GND

CE (pin 18) → VROM

Vector RAM

	3L 137211-001	3M 137211-001	3P 137211-001	4L 137211-001	4M 137211-001	4P 137211-001	
19						A10	
22						A9	
23						A8	
1						A7	
2						A6	
3						A5	
4						A4	
5						A3	
6						A2	
7						A1	
8						A0	
21						CWE	
D7						17	
D6						16	
D5						15	
D4						14	
D3						13	
:2						11	
D1						10	
D0						9	
CE	OE	CE	OE	CE	OE	CE	OE
10	20	10	20	10	20	10	20
VRAM0	VRAM1	VRAM2	VRAM3	VRAM4	VRAM5		

DVG7

DVG6

DVG5

DVG4

DVG3

DVG2

DVG1

DVG0

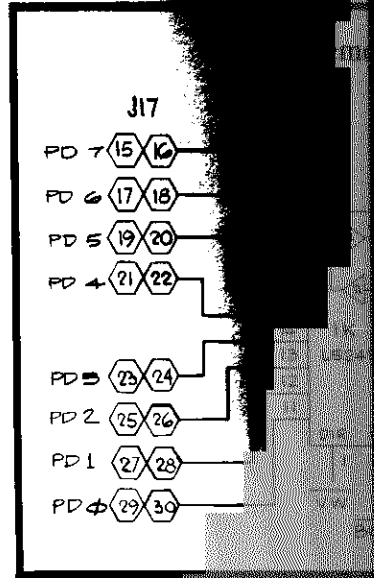
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The diagram illustrates the internal circuitry of a Vector Interface Buffer. It features an LS244 buffer with inputs connected to J17 pins and outputs connected to various system signals. The buffer is powered by 1G and 2G pins connected to ground. Logic gates (504, 5P, 3A, LS00) are used to generate control signals like VGHALT, VMEM, and VW.



Vector Address Selector

The figure illustrates four circuit diagrams for a Vector Address Selector, all powered by a +5V supply through a 10K resistor (R1) and a 5P capacitor (5P).

Top Left Circuit (LS244): This circuit uses an LS244 buffer. The inputs are J17 (R/WB, AB13, AB12, AB11, AB10, AB9, AB8) and P, R109. The output is AM13, AM12, AM11, AM10, AM9, and AM8. The buffer is powered by VMEM.

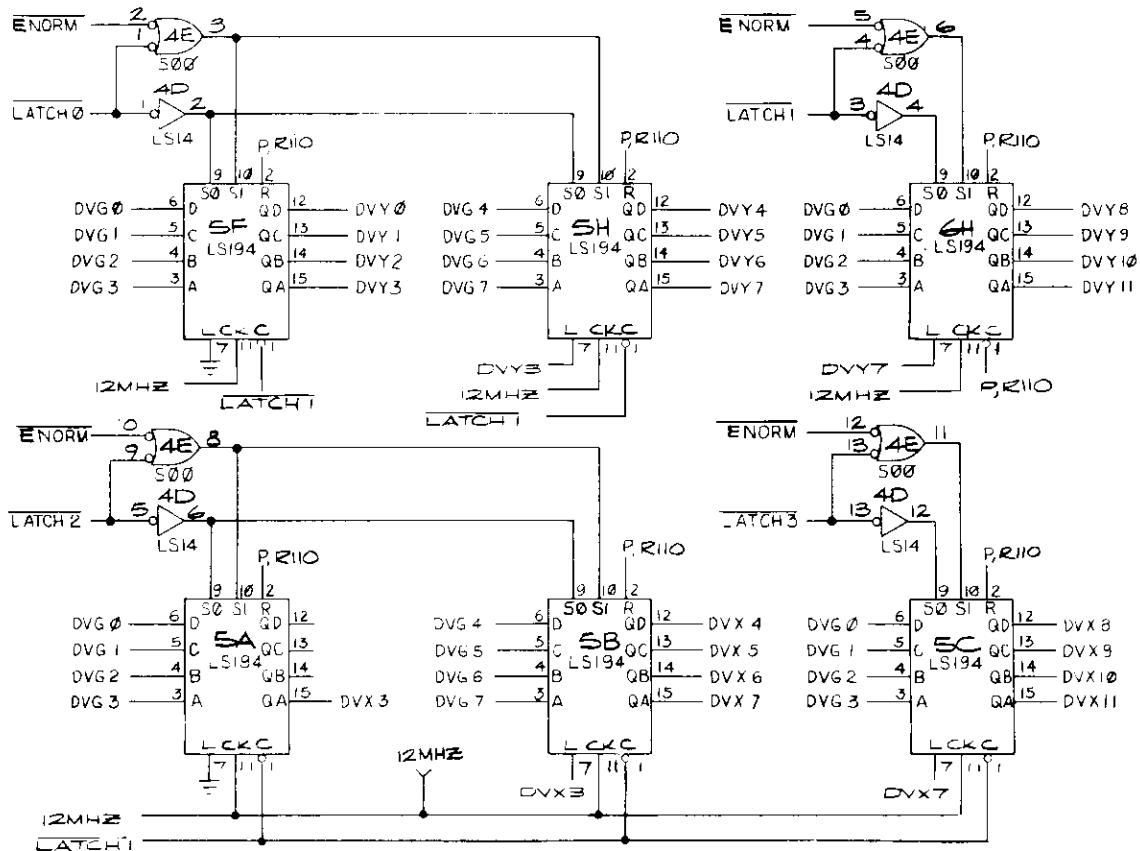
Top Right Circuit (2N LS244): This circuit uses a 2N LS244 buffer. The inputs are P, R109 (AVG13, AVG12, AVG11, AVG10, AVG9, AVG8) and P, R109. The output is AM13, AM12, AM11, AM10, AM9, and AM8. The buffer is powered by VMEM.

Bottom Left Circuit (1M LS244): This circuit uses a 1M LS244 buffer. The inputs are AB7, AB6, AB5, AB4, AB3, AB2, AB1, and AB0. The output is AM7, AM6, AM5, AM4, AM3, AM2, AM1, and AM0. The buffer is powered by VMEM.

Bottom Right Circuit (2M LS244): This circuit uses a 2M LS244 buffer. The inputs are AVG7, AVG6, AVG5, AVG4, AVG3, AVG2, AVG1, and AVG0. The output is AM7, AM6, AM5, AM4, AM3, AM2, AM1, and AM0. The buffer is powered by VMEM.



Vector Data Shifters



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STAR WARS Analog Vector-Generator PCB

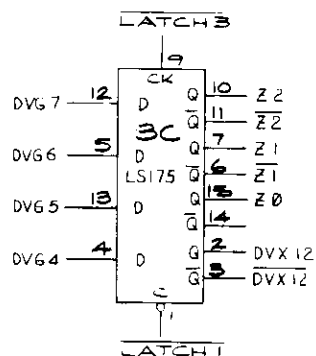
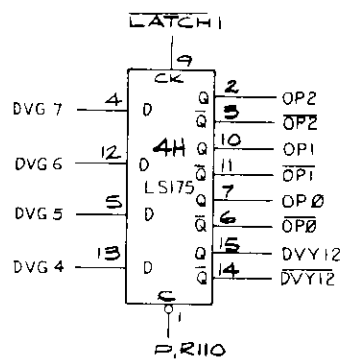


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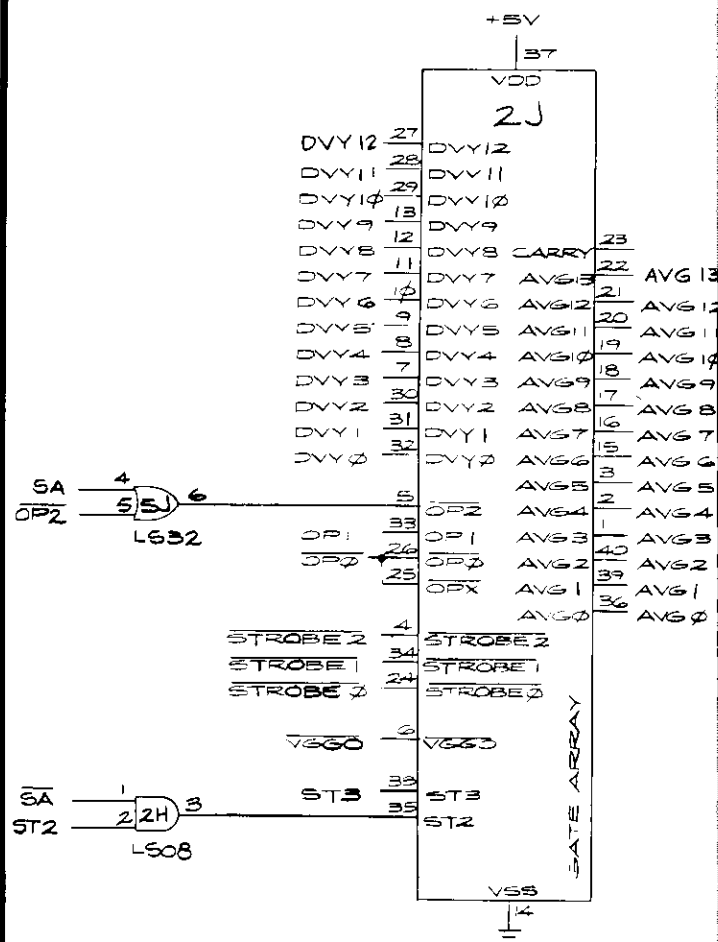
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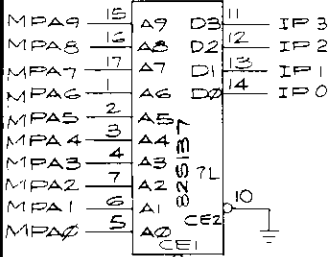
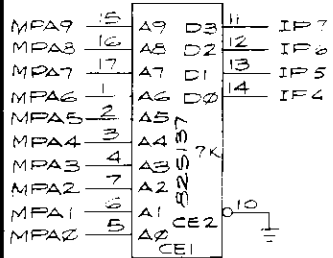
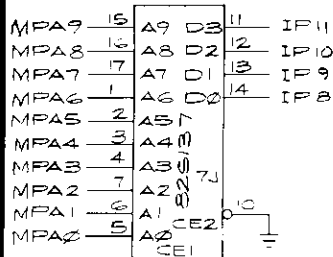
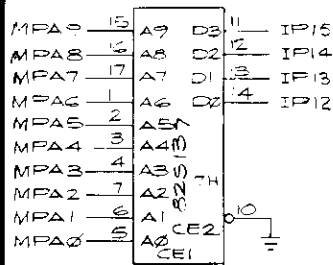
Op Code and Intensity Latches



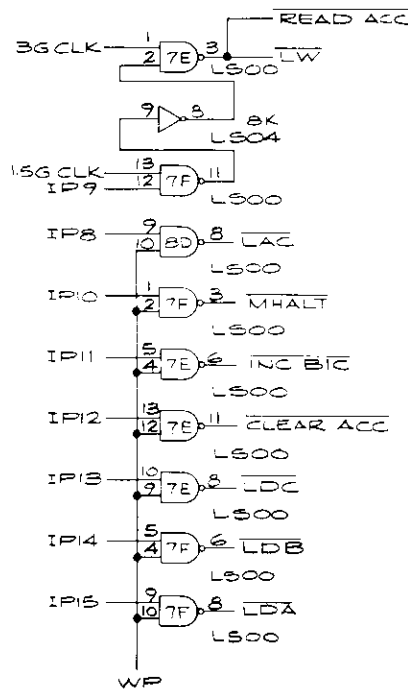
Address Controller



Instruction PROM



Instruction Strobe Gates



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STAR WARS Main PCB

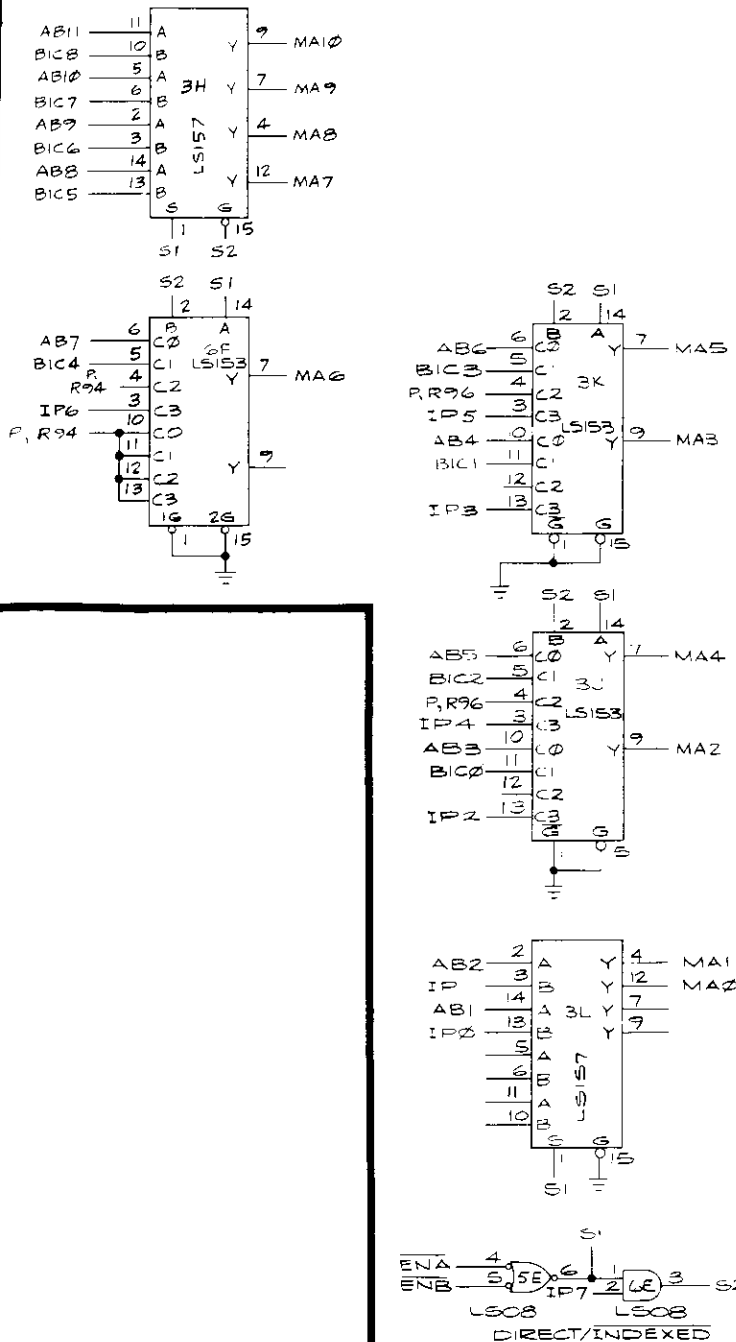


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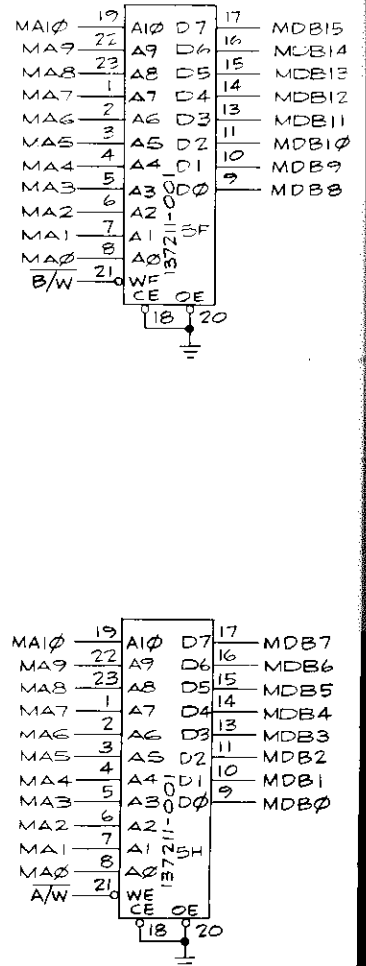
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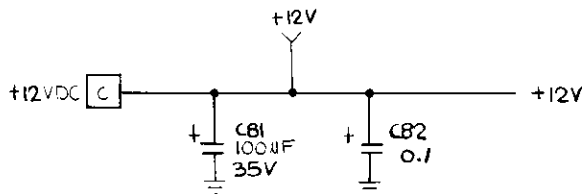
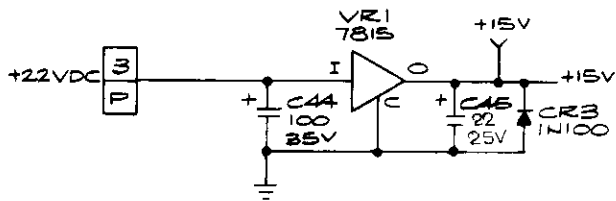
Matrix Processor Address Selector



Matrix Processor RAM



Power Input



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STAR WARS Analog Vector-Generator PCB

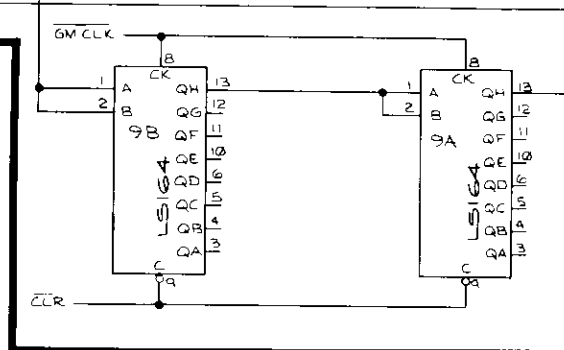
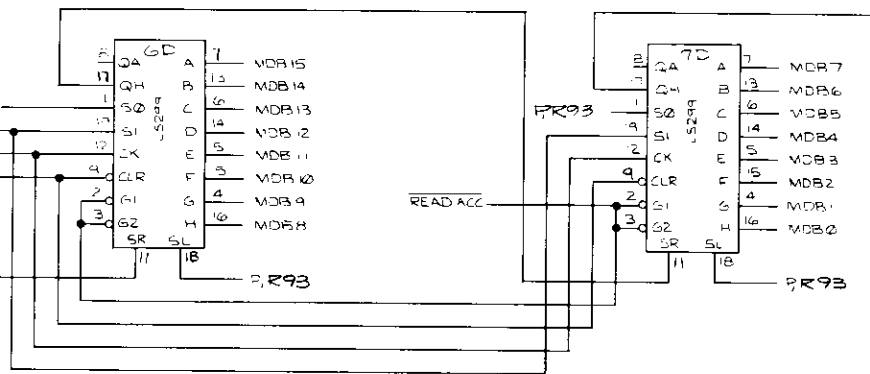


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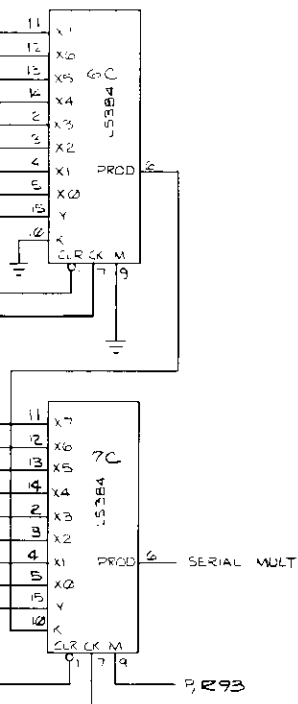
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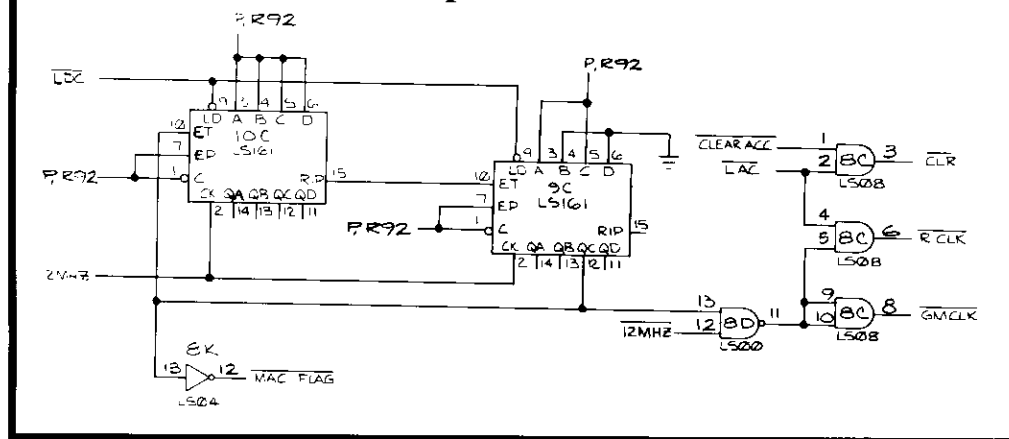
Accumulator



al Multiplier



Multiplier/Accumulator Clock



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STAR WARS Main PCB

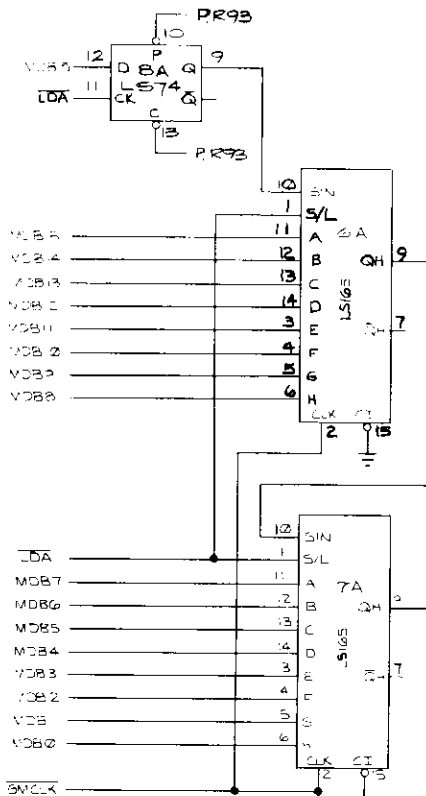


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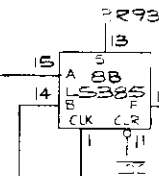
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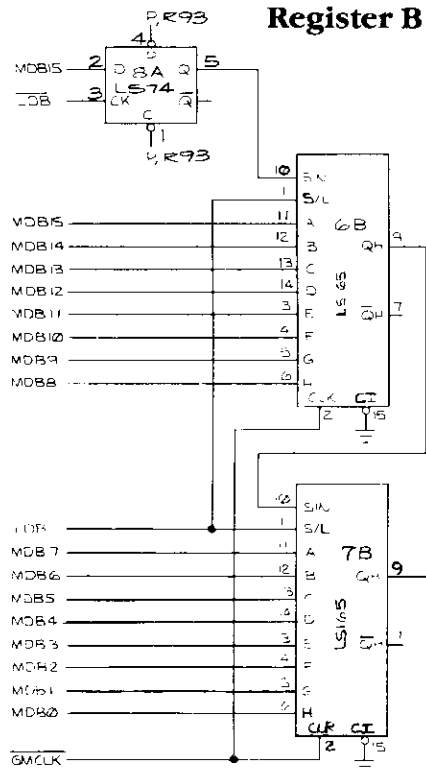
Register A



Serial Subtractor



Register B

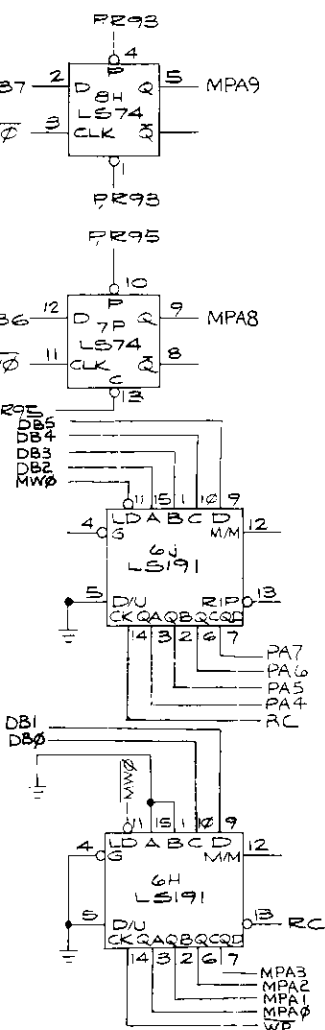


Serial

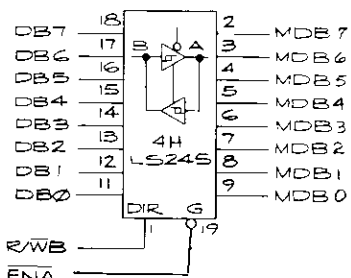
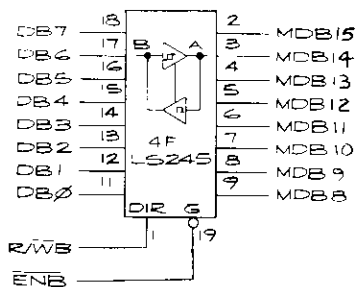
MDB15
MDB14
MDB13
MDB12
MDB11
MDB10
MDB9
MDB8

MDB7
MDB6
MDB5
MDB4
MDB3
MDB2
MDB1
MDB0

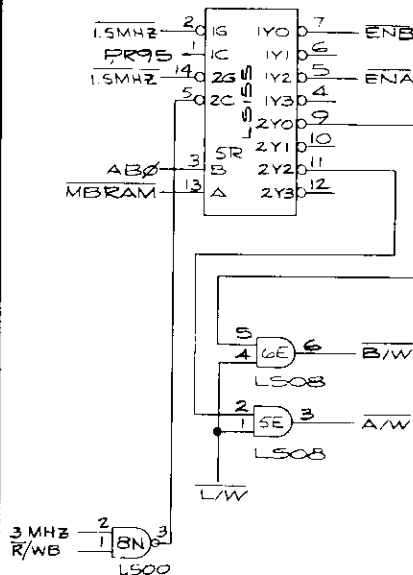
Matrix Processor Address Counter



Matrix Processor Data Selector



Matrix Processor Address and Data Selector Control



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STAR WARS Main PCB



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Matrix Processor Clock

The diagram illustrates the timing for the Matrix Processor Clock. It features a 2 MHz clock source connected to a 74LS161 counter (P, R92) and a 74LS74 flip-flop (MHALT). The counter's Q0-Q3 outputs are connected to a 74LS10 NAND gate (S02) and a 74LS13 inverter (S02). The flip-flop's Q output is connected to a 74LS10 NAND gate (S02) and a 74LS13 inverter (S02). The output of the NAND gate is connected to the clock input of the flip-flop. The output of the inverter is connected to the clock input of the counter. The output of the counter is connected to the clock input of the flip-flop. The output of the flip-flop is connected to the clock input of the counter. The output of the counter is connected to the clock input of the flip-flop. The output of the flip-flop is connected to the clock input of the counter.

Block Index Counter

The diagram illustrates a Block Index Counter circuit using two LSI 91 chips. The circuit is powered by a 5V supply and includes several control and data lines.

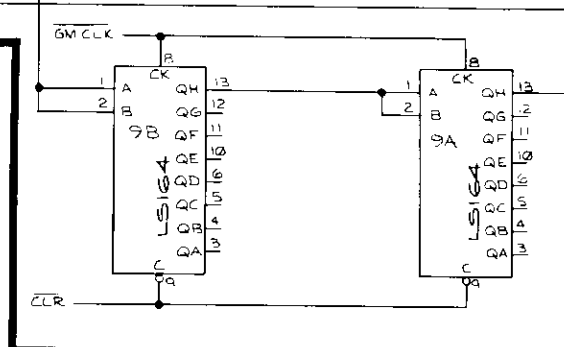
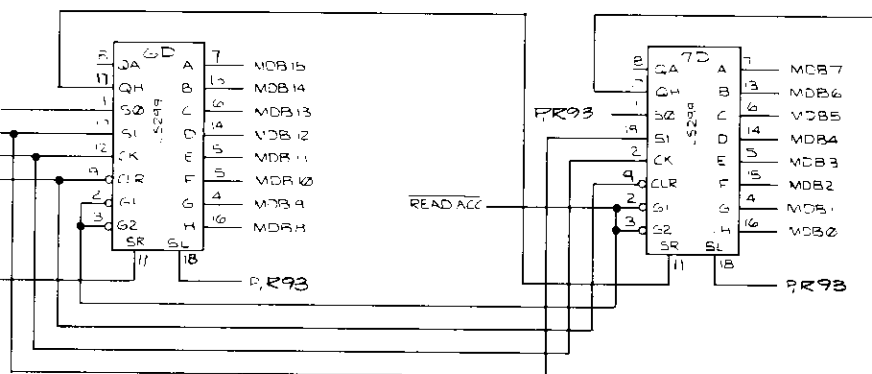
Top LSI 91 Chip:

- Inputs:** DB7, DB6, DB5, DB4, MW2, INCBIC.
- Outputs:** BIC7, BIC6, BIC5, BIC4.
- Internal Connections:** LD (pin 11) to DB7; A (pin 15) to DB6; B (pin 1) to DB5; C (pin 10) to DB4; D (pin 9) to MW2. LD (pin 4) is grounded. G (pin 3) is connected to INCBIC. F (pin 12) is connected to BIC7. M (pin 13) is connected to BIC6. M (pin 13) is also connected to the D/U input (pin 14) of the bottom chip. CK (pin 1) is grounded. QA (pin 2), QB (pin 3), QC (pin 6), and QD (pin 7) are connected to BIC5, BIC4, BIC3, and BIC2 respectively.

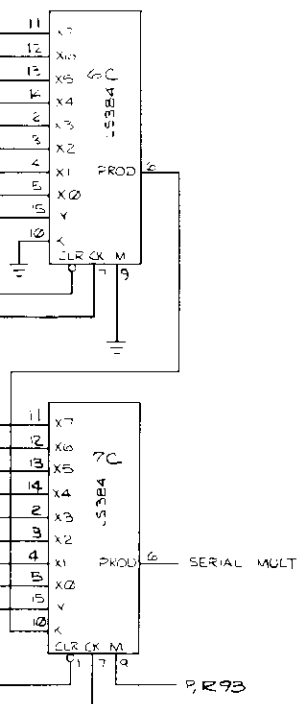
Bottom LSI 91 Chip:

- Inputs:** DB3, DB2, DB1, DB0, INCBIC.
- Outputs:** BIC3, BIC2, BIC1, BIC0.
- Internal Connections:** LD (pin 11) to DB3; A (pin 15) to DB2; B (pin 1) to DB1; C (pin 10) to DB0; D (pin 9) to DB0. LD (pin 4) is grounded. G (pin 3) is connected to INCBIC. F (pin 12) is connected to BIC3. M (pin 13) is connected to BIC2. M (pin 13) is also connected to the D/U input (pin 14) of the top chip. CK (pin 1) is grounded. QA (pin 2), QB (pin 3), QC (pin 6), and QD (pin 7) are connected to BIC1, BIC0, BIC3, and BIC2 respectively.

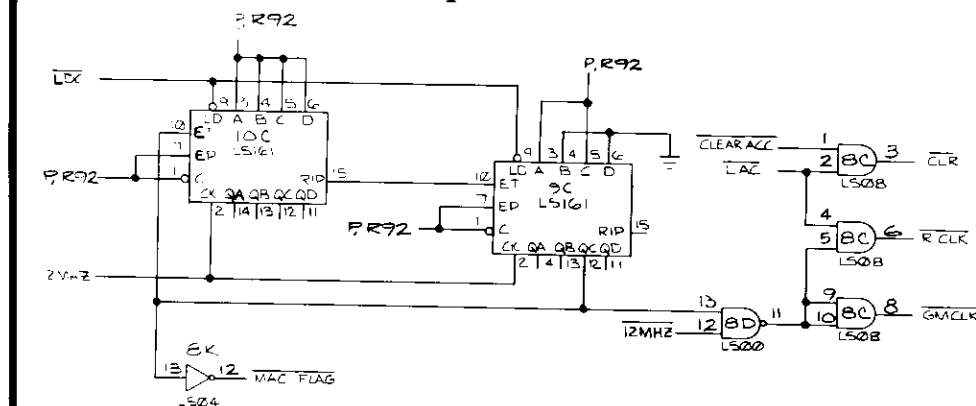
Accumulator



al Multiplier



Multiplier/Accumulator Clock



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STAR WARS Main PCB



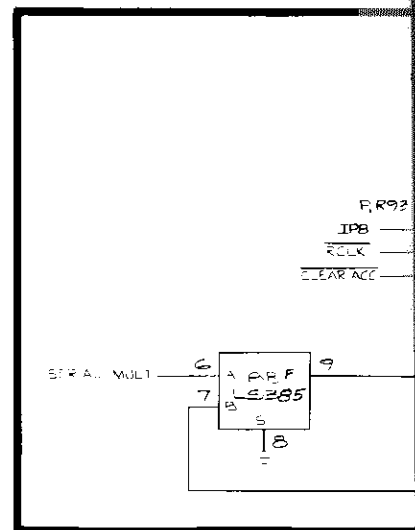
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Register A

The diagram shows the internal logic of Register A. It consists of a 74LS74 flip-flop and two 74LS163 counters. The flip-flop is clocked by PR9B and its Q output is connected to the clock of the first 74LS163 counter. The first counter's outputs (A-H) are connected to MOB15 through MOB8. The second 74LS163 counter is clocked by the output of the first counter (pin 9) and its outputs (A-H) are connected to MOB7 through MOB0. Both counters have their S/L pins connected to LDA and their CK pins connected to SWCLK. The QH pin of the second counter is connected to pin 7.

[illegible]

Serial

MCB15	_____
MCB14	_____
MCB13	_____
MCB12	_____
MCB11	_____
MCB10	_____
MCB9	_____
MCB8	_____

-DC _____ ●

MCB7	_____
MCB6	_____
MCB5	_____
MCB4	_____
MCB3	_____
MCB2	_____
MCB1	_____
MCB0	_____

der

14

15

2

6

9

4

5

2

6

9

14

15

2

6

9

14

15

2

6

9

14

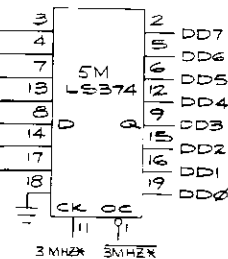
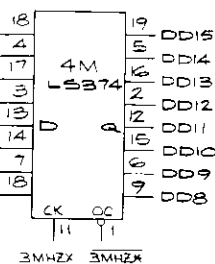
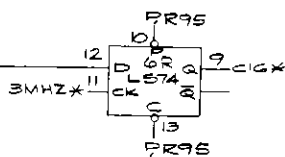
15

2

6

9

Difference Latch



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STAR WARS Main PCB

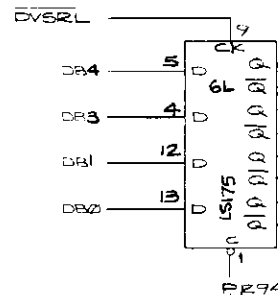
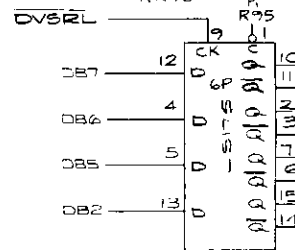
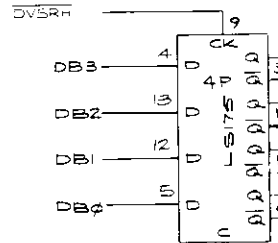
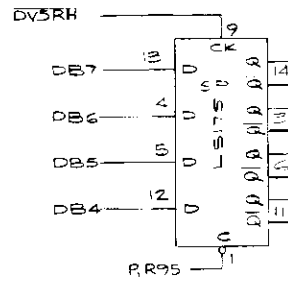


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Divisor Inverting Latch



DD15	16	B4	C4
DD14	15	A4	Z4
DD13	14	B3	M
DD12	13	A3	M
DD11	12	B2	M
DD10	11	A2	M
DD9	10	B1	J
DD8	9	A1	M
DD7	8	C0	SN

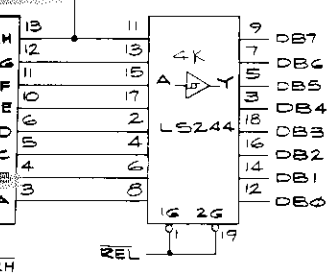
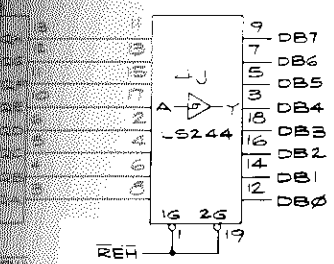
DD11	16	B4	C4
DD10	15	A4	Z4
DD9	14	B3	M
DD8	13	A3	M
DD7	12	B2	M
DD6	11	A2	M
DD5	10	B1	J
DD4	9	A1	M
DD3	8	C0	4N

DD7	16	B4	C4
DD6	15	A4	Z4
DD5	14	B3	M
DD4	13	A3	M
DD3	12	B2	M
DD2	11	A2	M
DD1	10	B1	J
DD0	9	A1	M
DD15	8	C0	6N

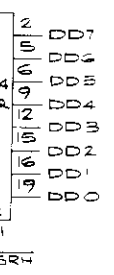
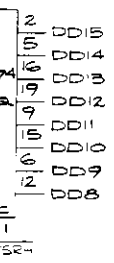
DD3	16	B4	C4
DD2	15	A4	Z4
DD1	14	B3	M
DD0	13	A3	M
DD15	12	B2	M
DD14	11	A2	M
DD13	10	B1	J
DD12	9	A1	M
DD11	8	C0	6M

P, R94

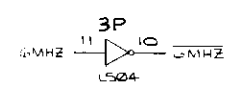
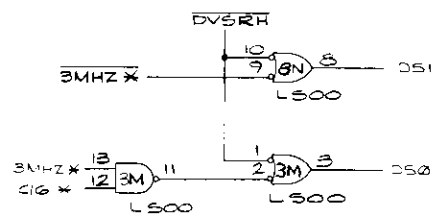
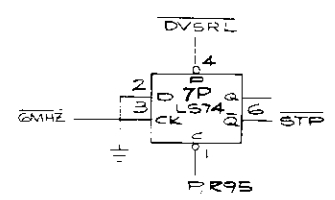
ient Shift Register



d Latch



Divider Control



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STAR WARS Main PCB

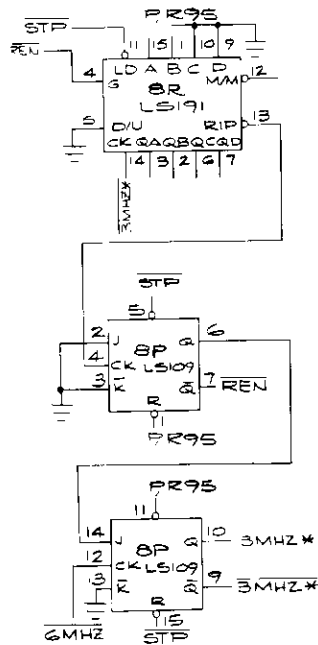


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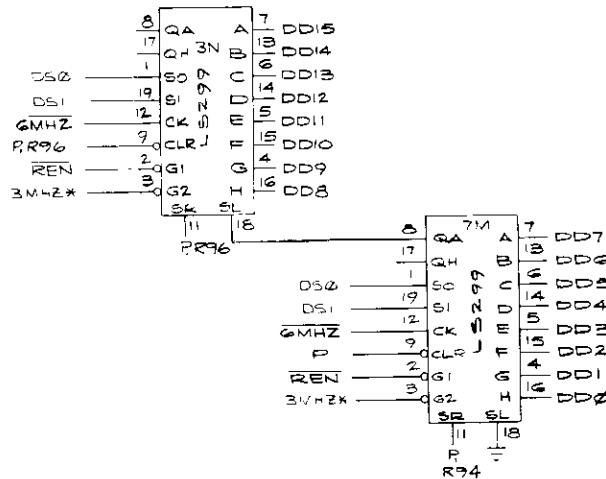
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SP-225 Sheet 1st page

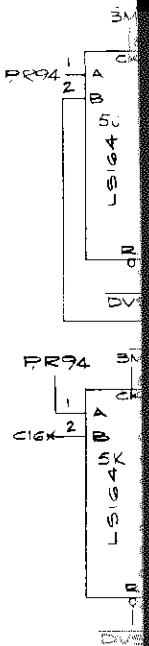
Divider Clock Generator



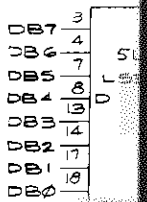
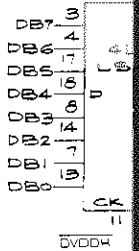
Dividend Shift Register



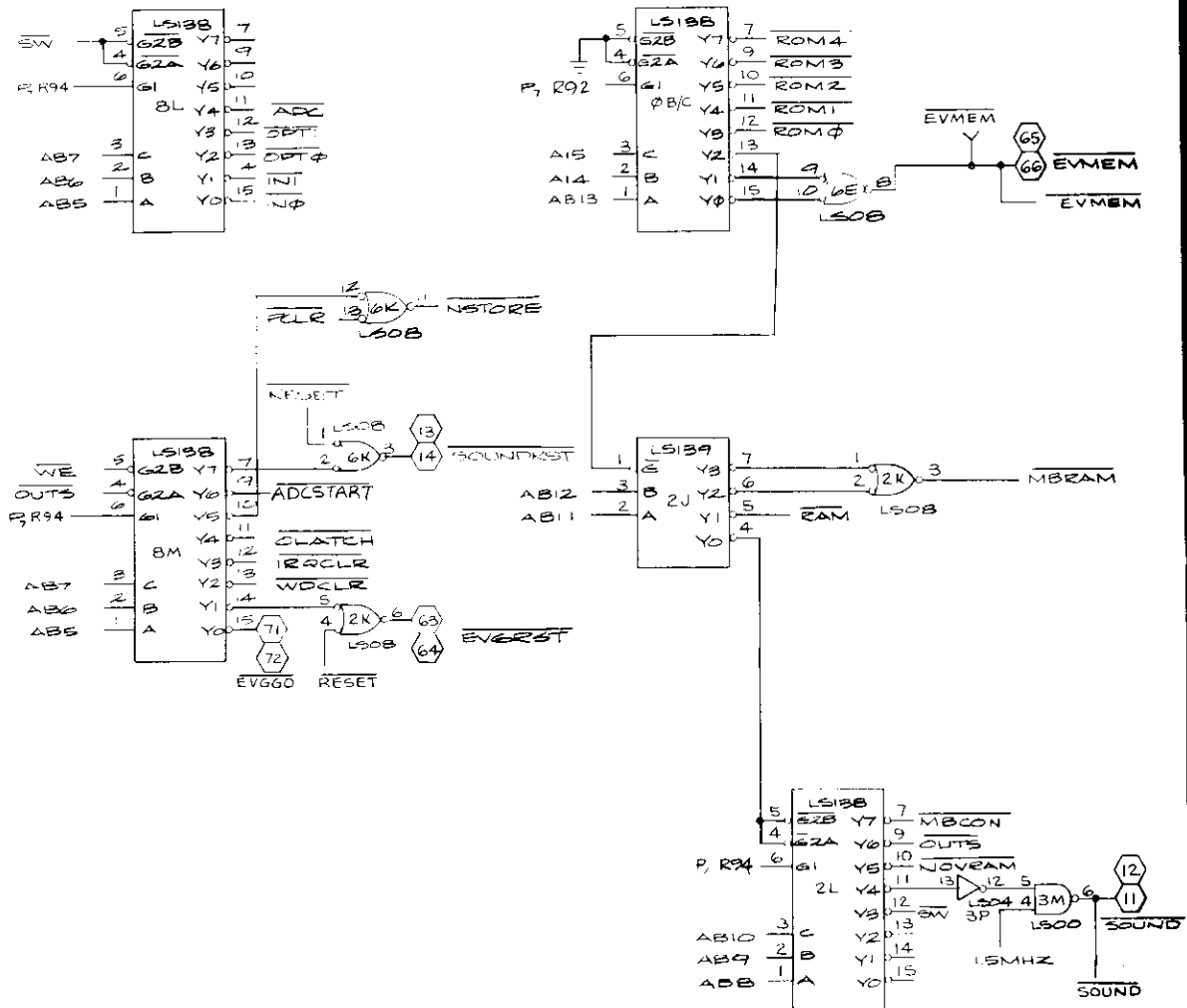
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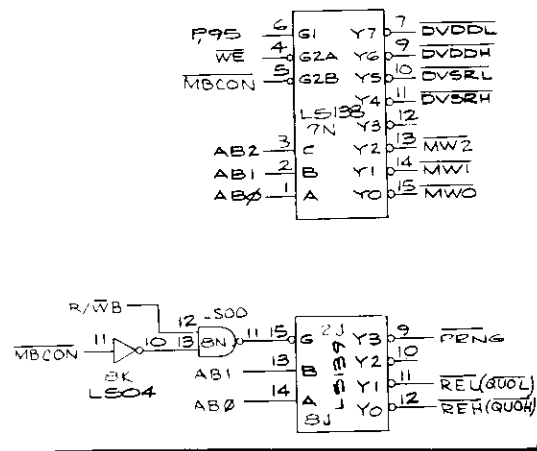
Dividen



Address Decoders



Math Address Decoders



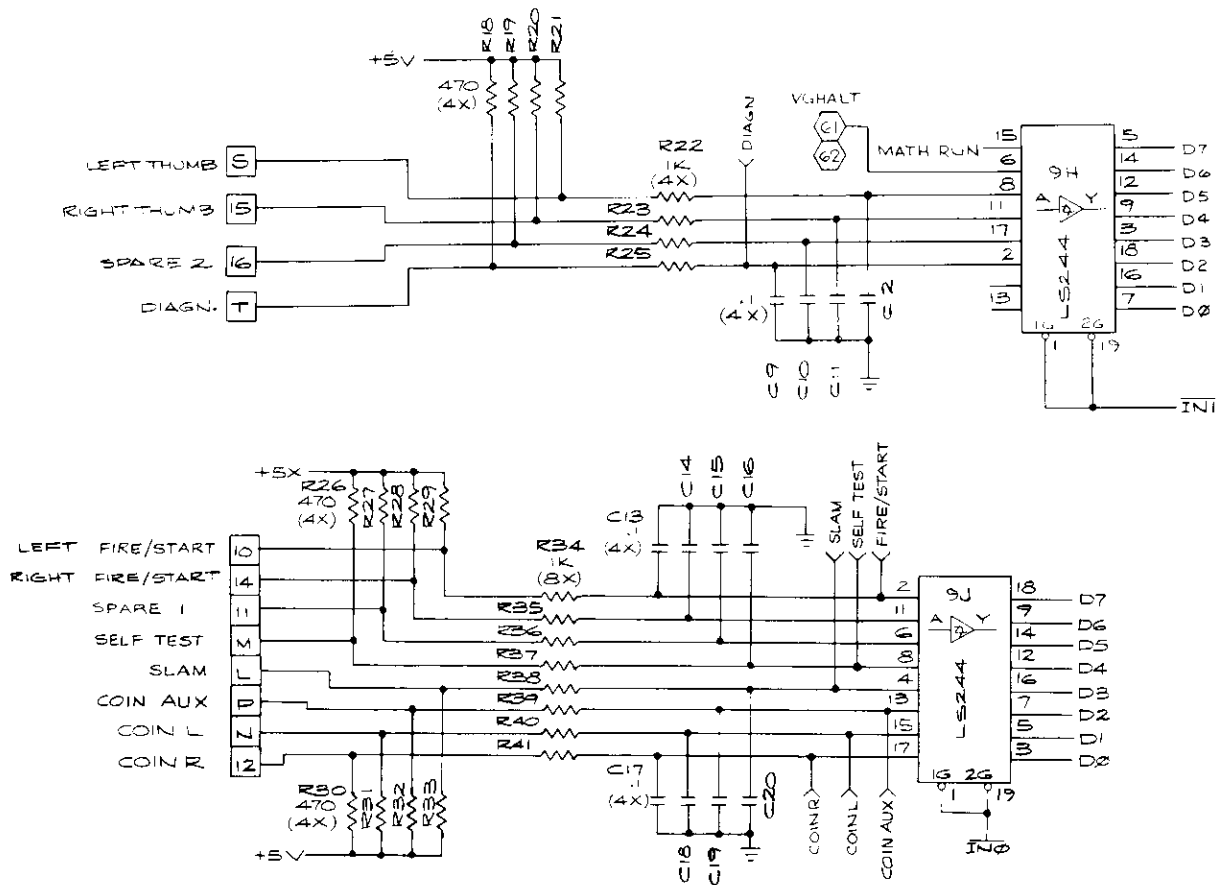
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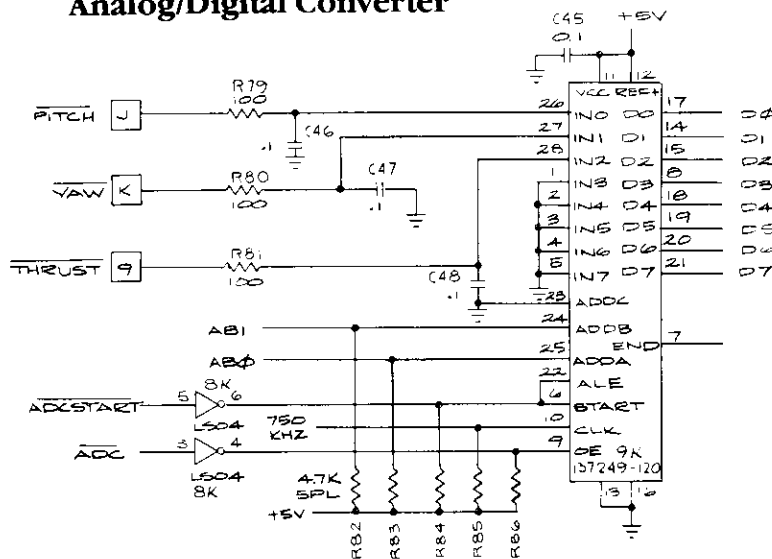
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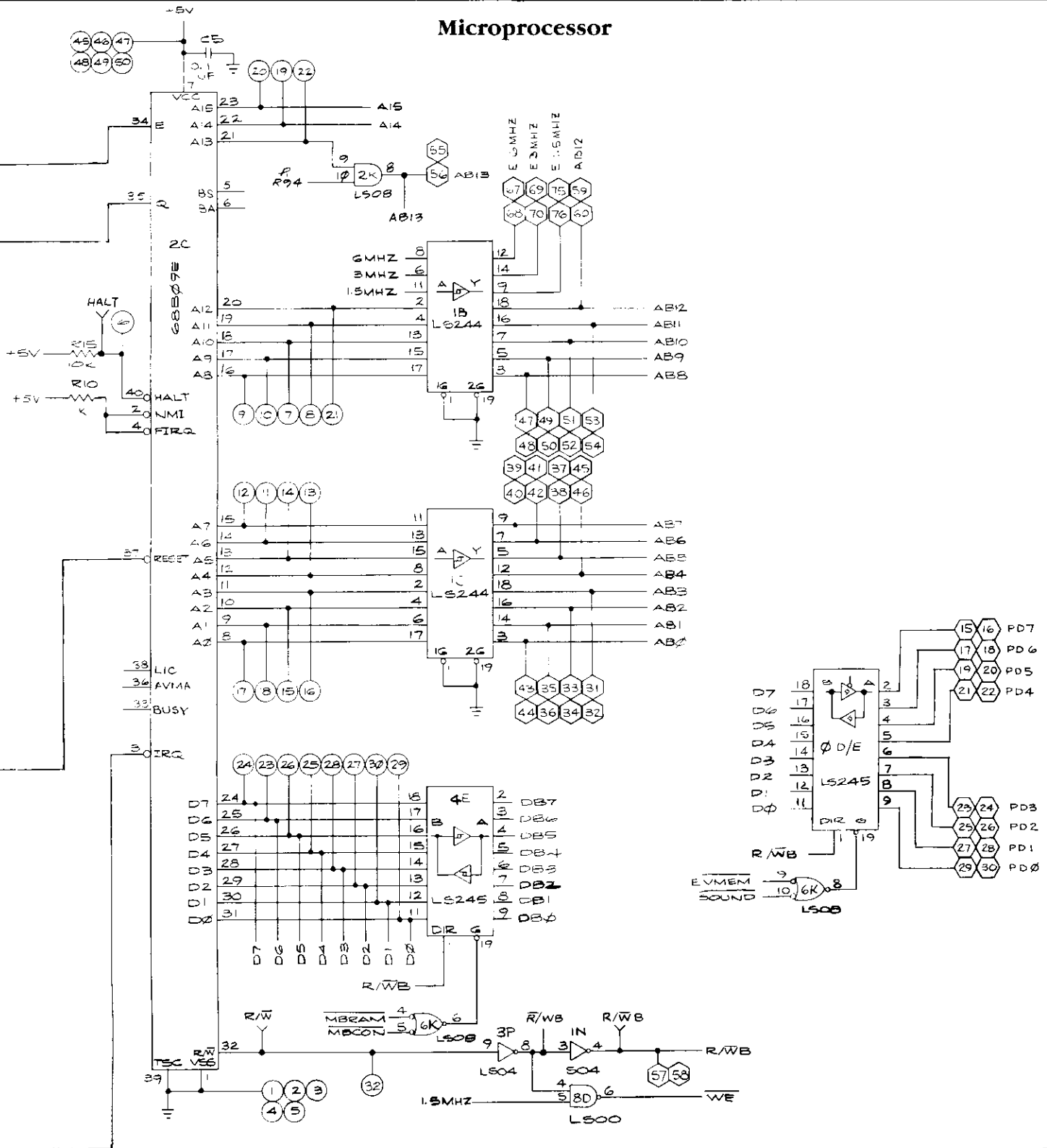
Coin Door and Control Panel Input



Analog/Digital Converter



Microprocessor



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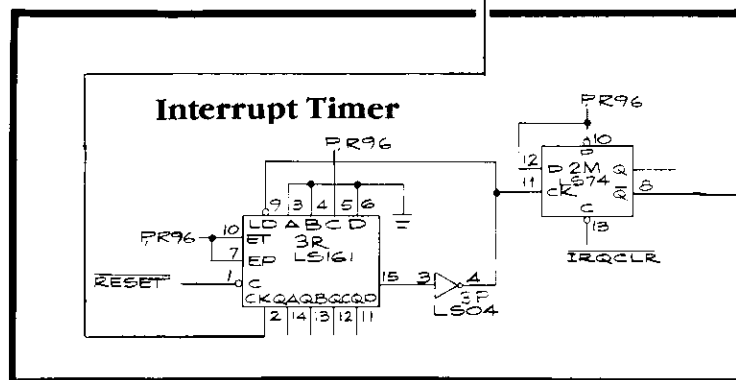
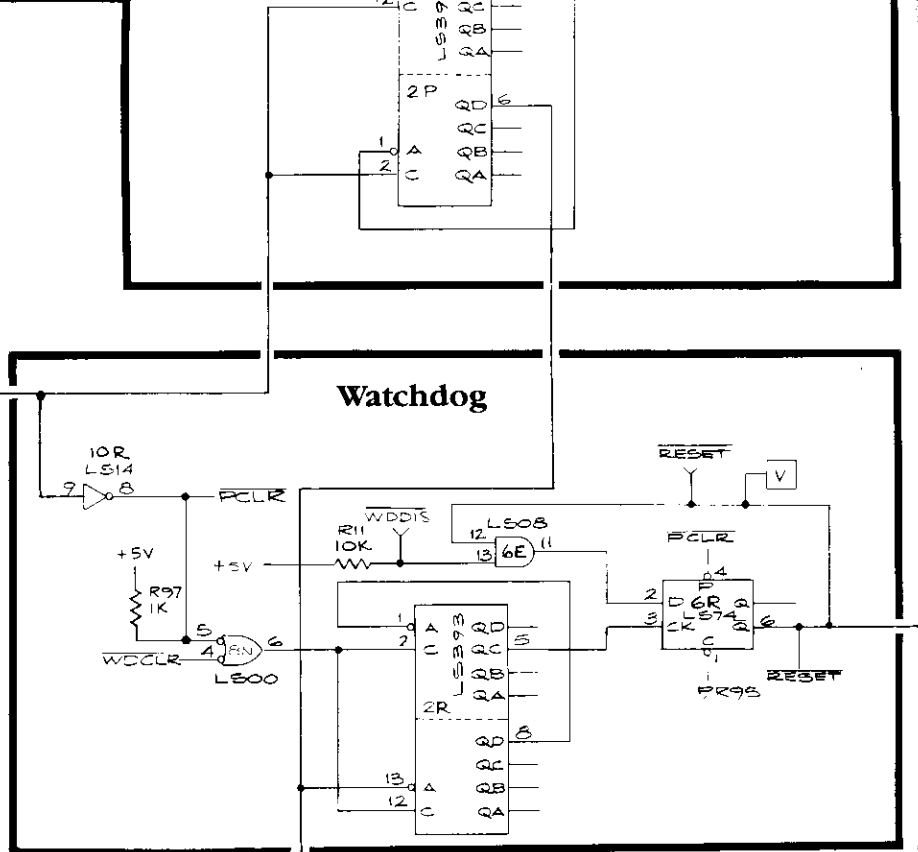
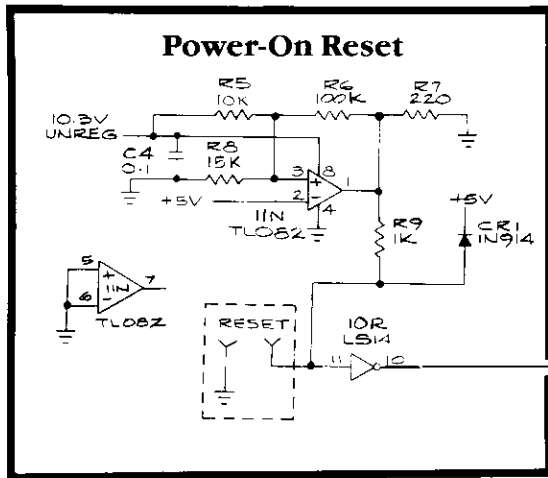
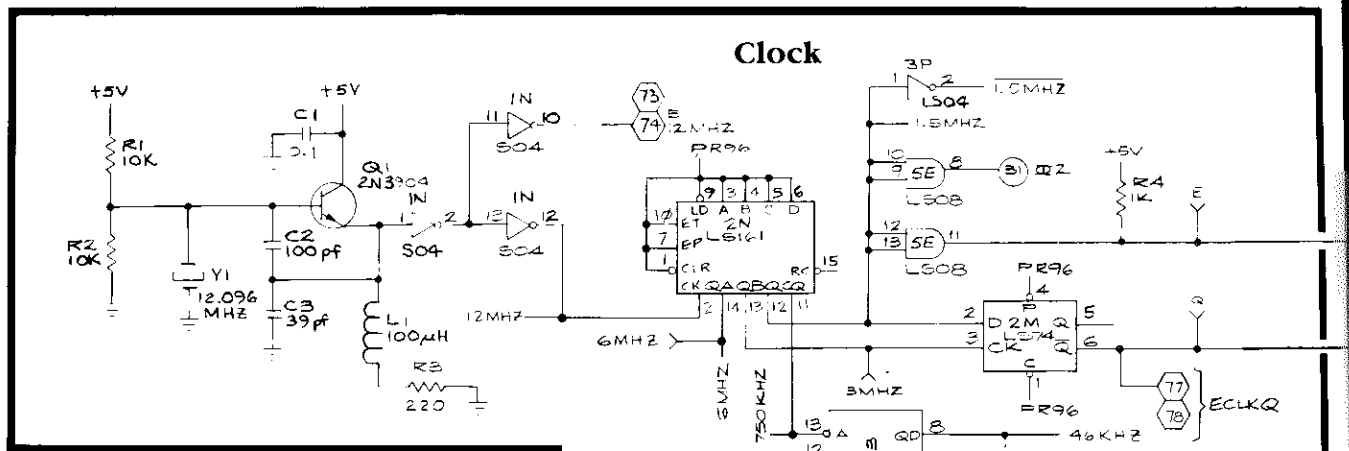
STAR WARS Main PCB



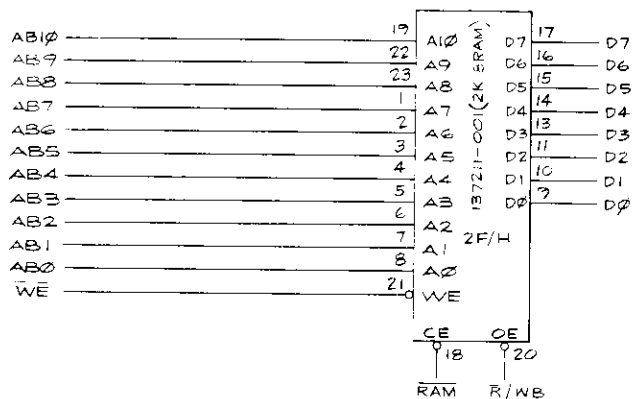
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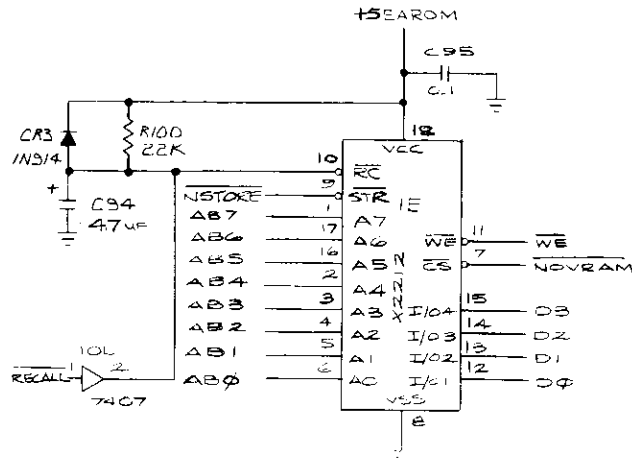
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RAM



High-Score and Bookkeeping Non-Volatile RAM



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STAR WARS Main PCB

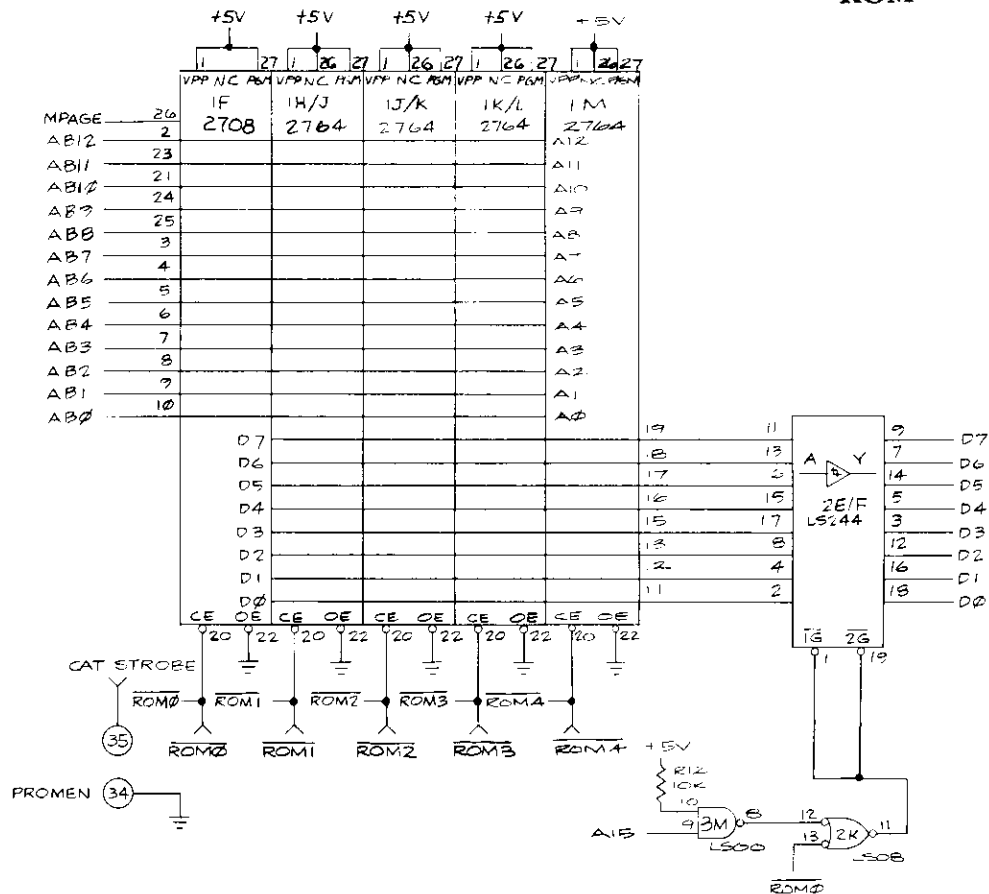


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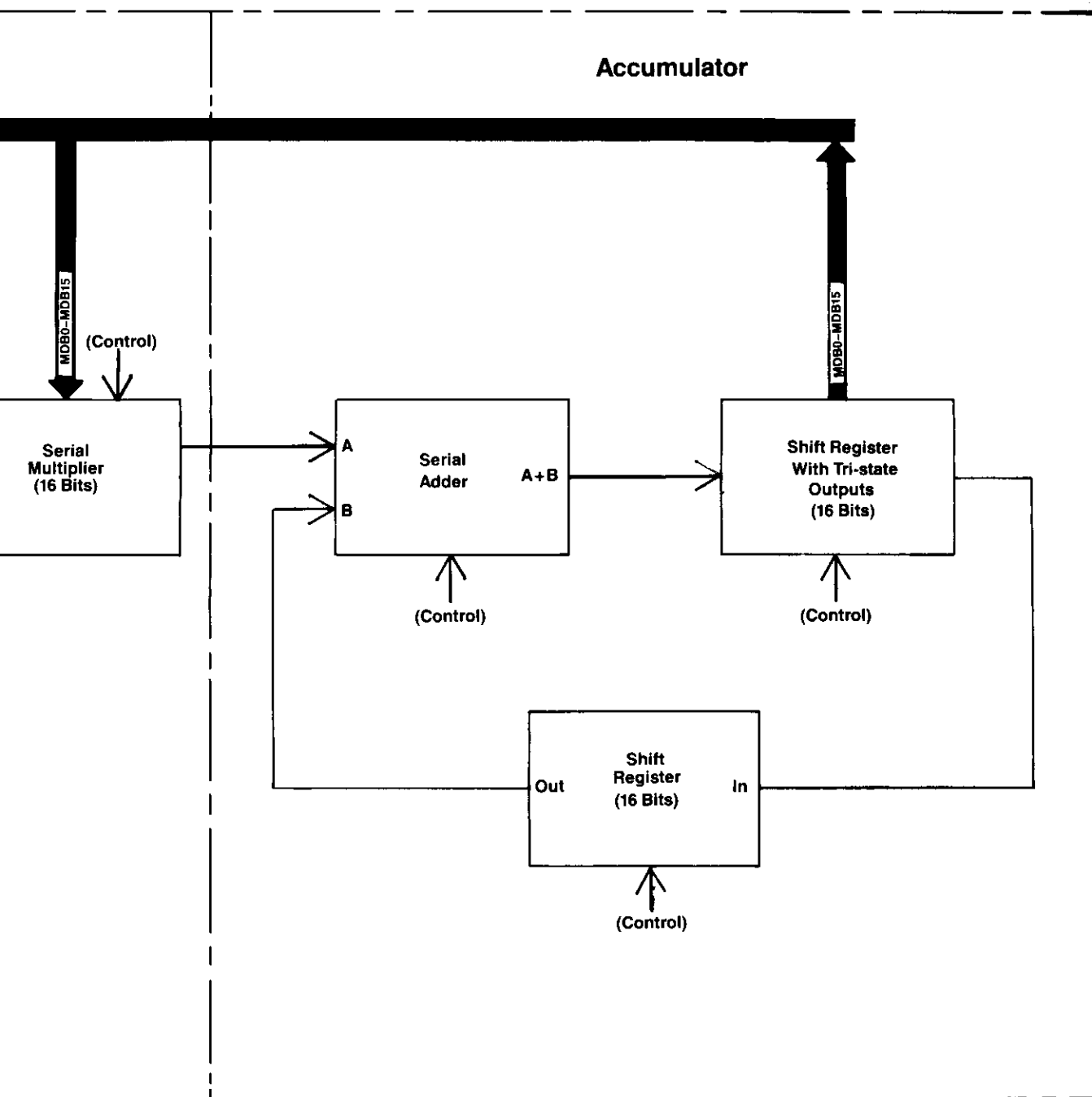
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ROM



ccumulator
+ (A-B) × C



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**STAR WARS Multiplier/Accumulator
Detailed Block Diagram**

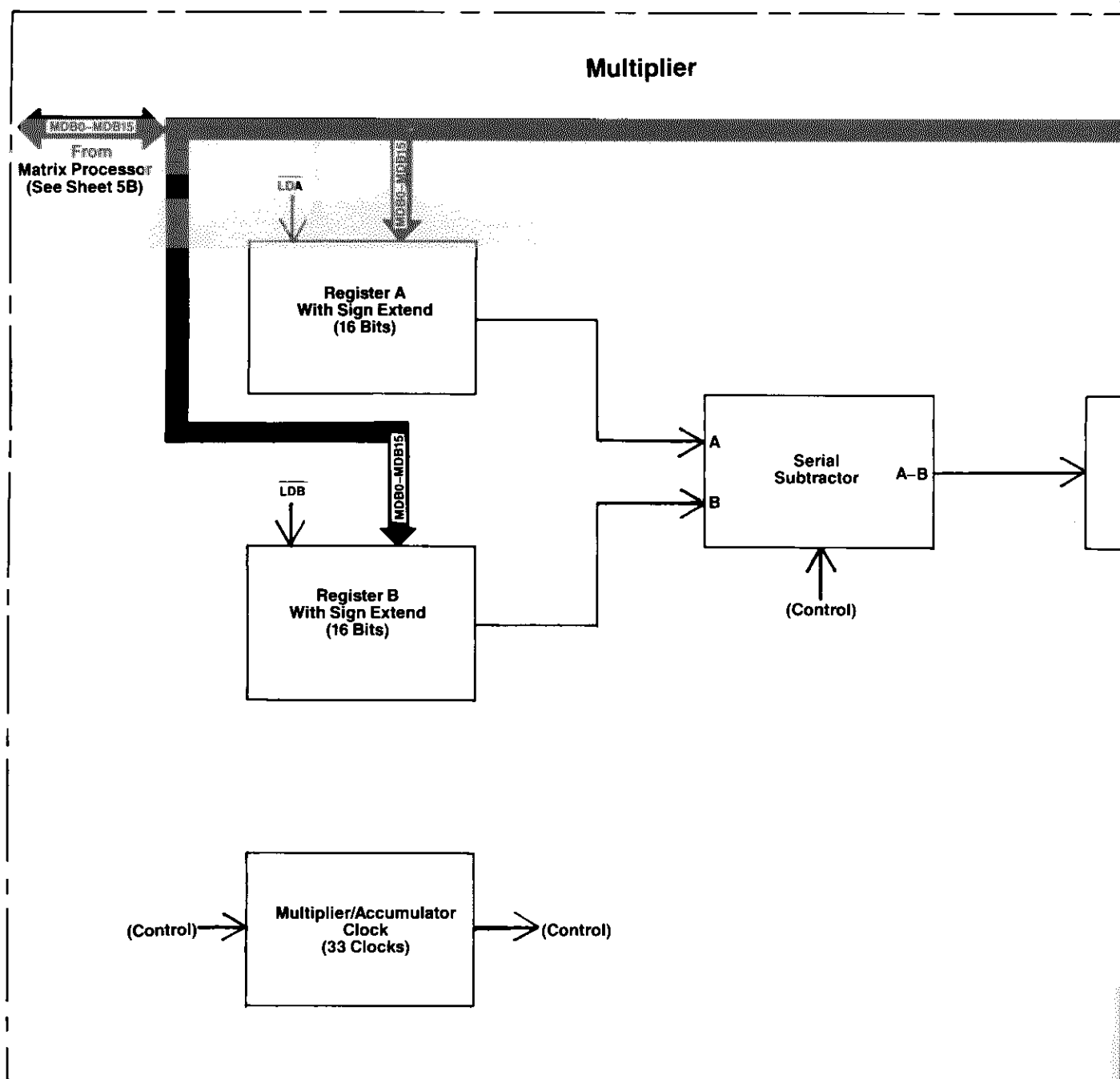


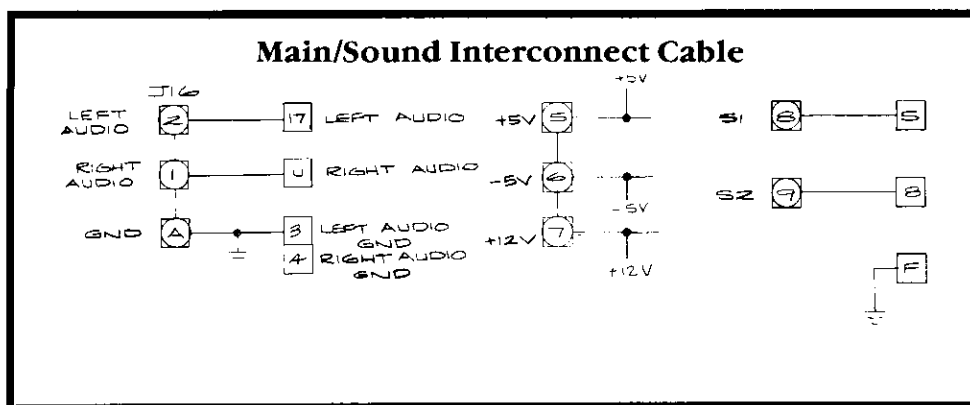
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Multiplier/
ACC = ACC





NOTE

- = J20 CONNECTOR
- = TEST CONNECTOR
- ◇ = J17 CONNECTOR
- ⊠ = J16 CONNECTOR

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STAR WARS Main PCB

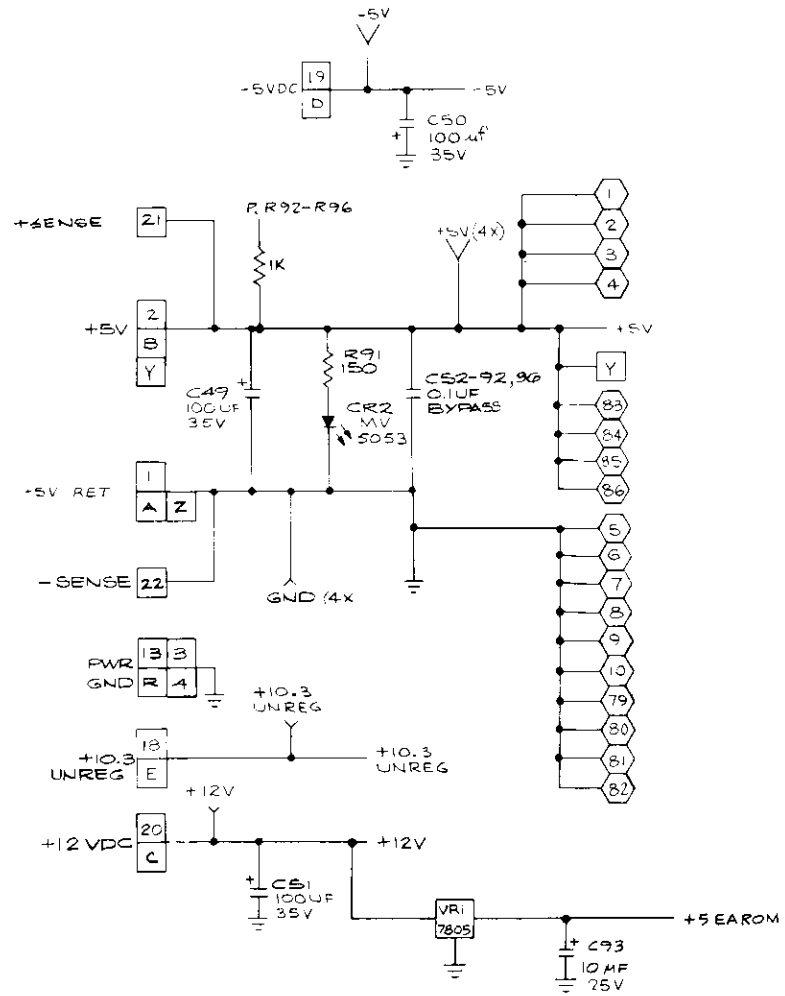


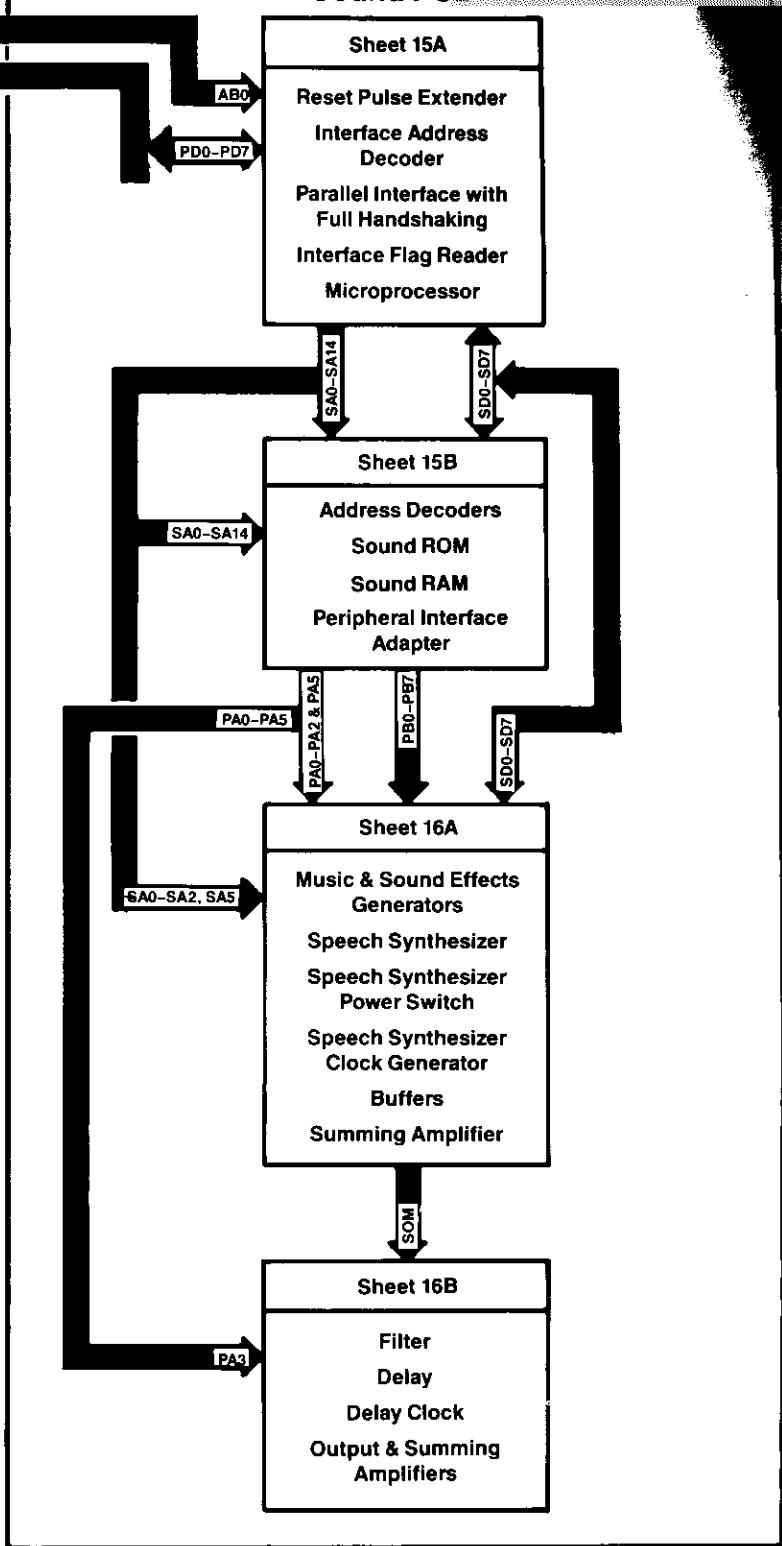
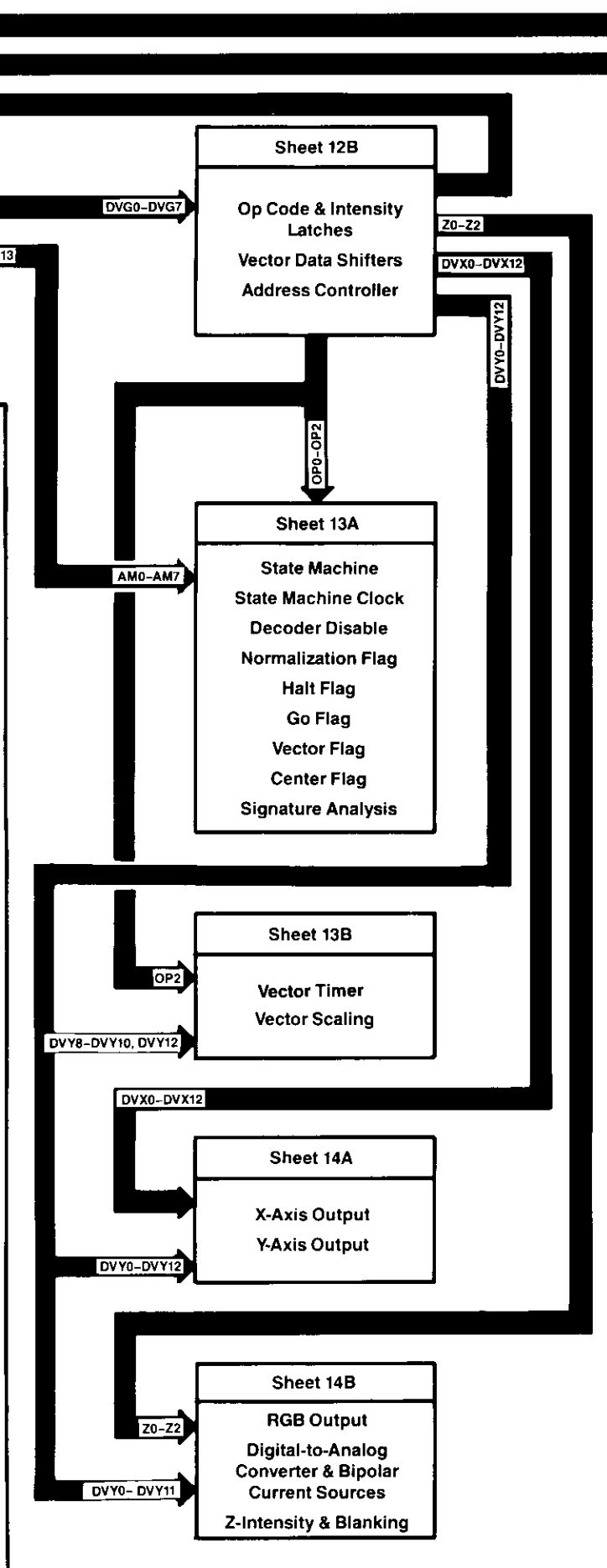
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Power Input





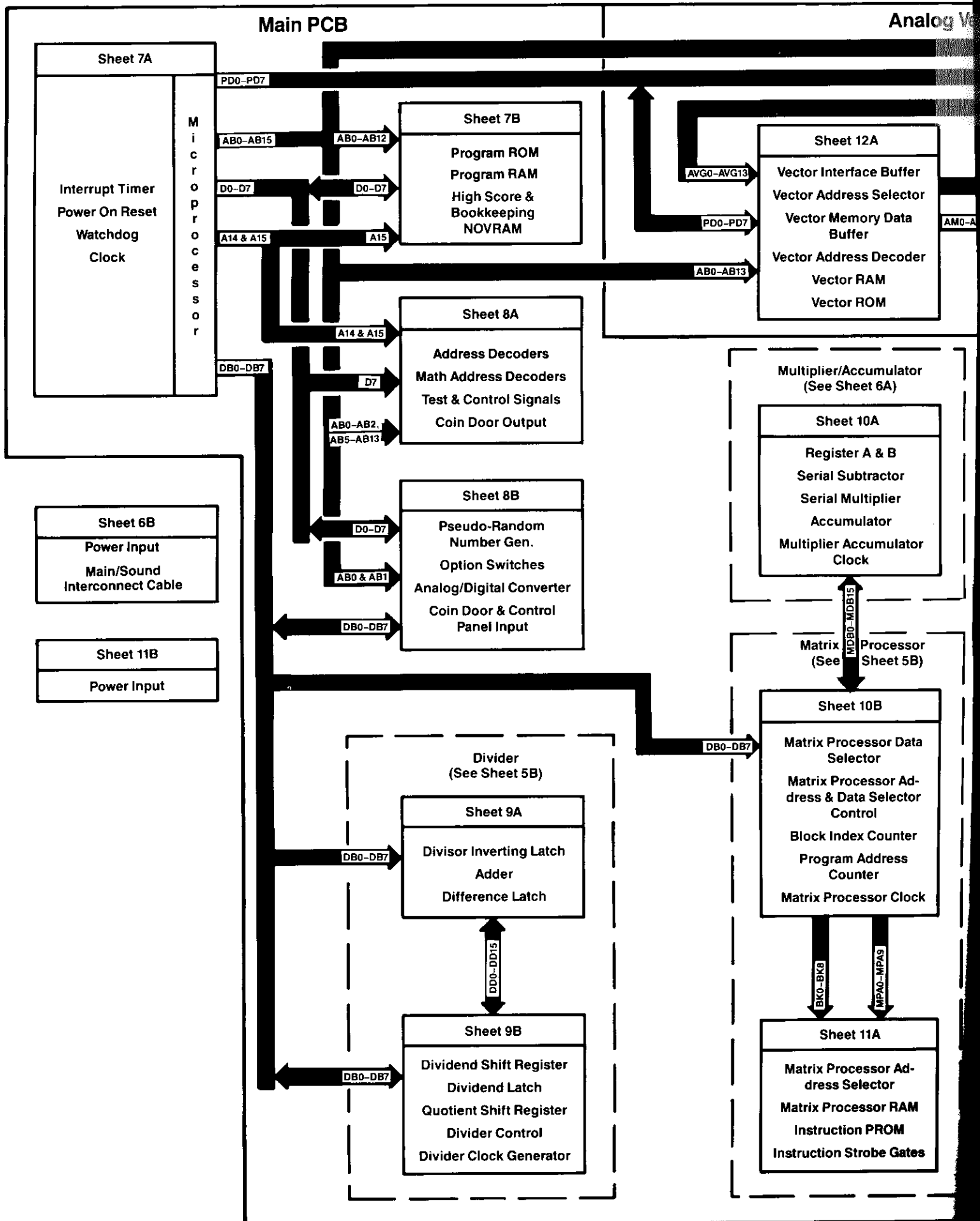
STAR WARS Functional Block Diagram and Guide to PCB Schematics

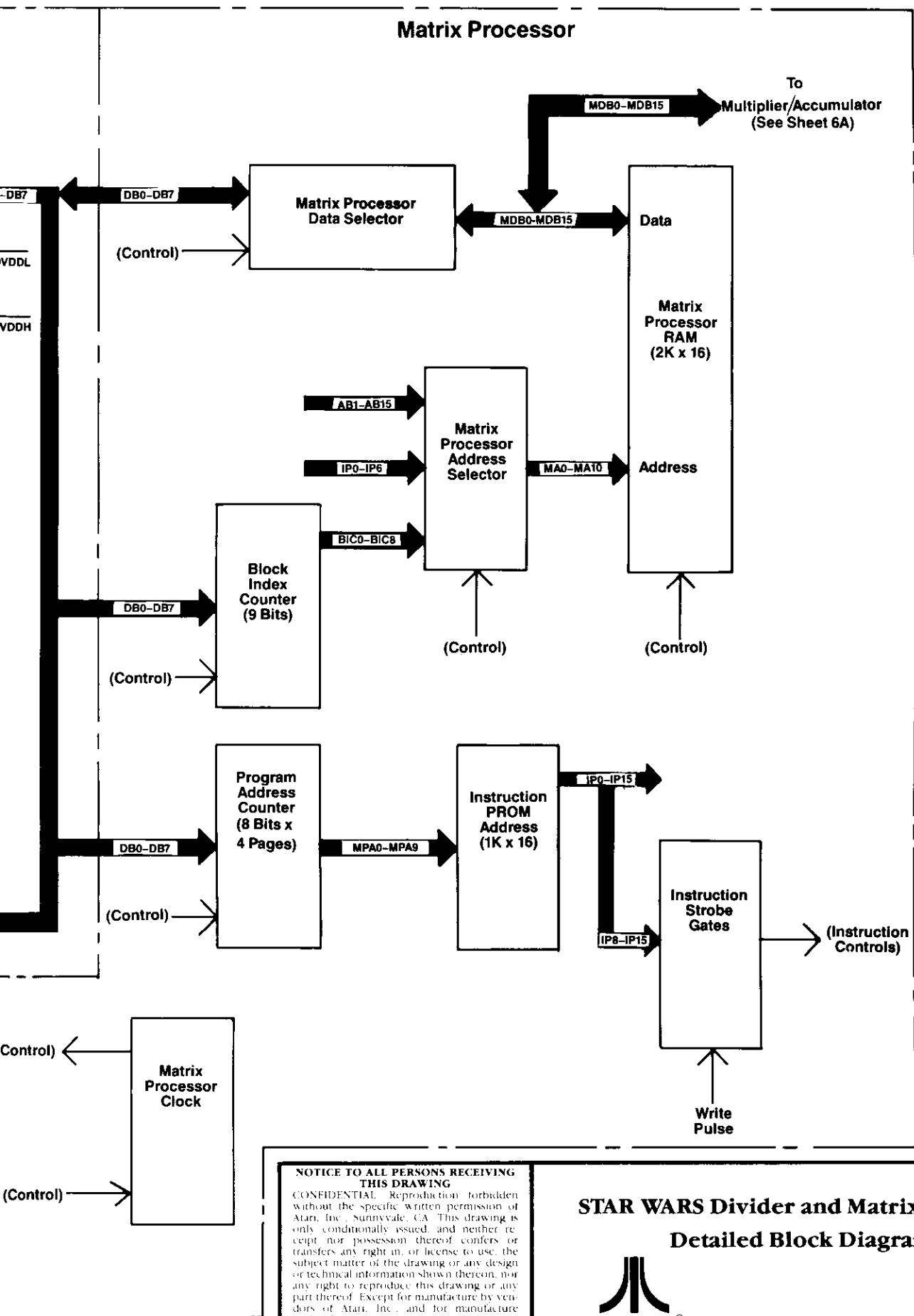


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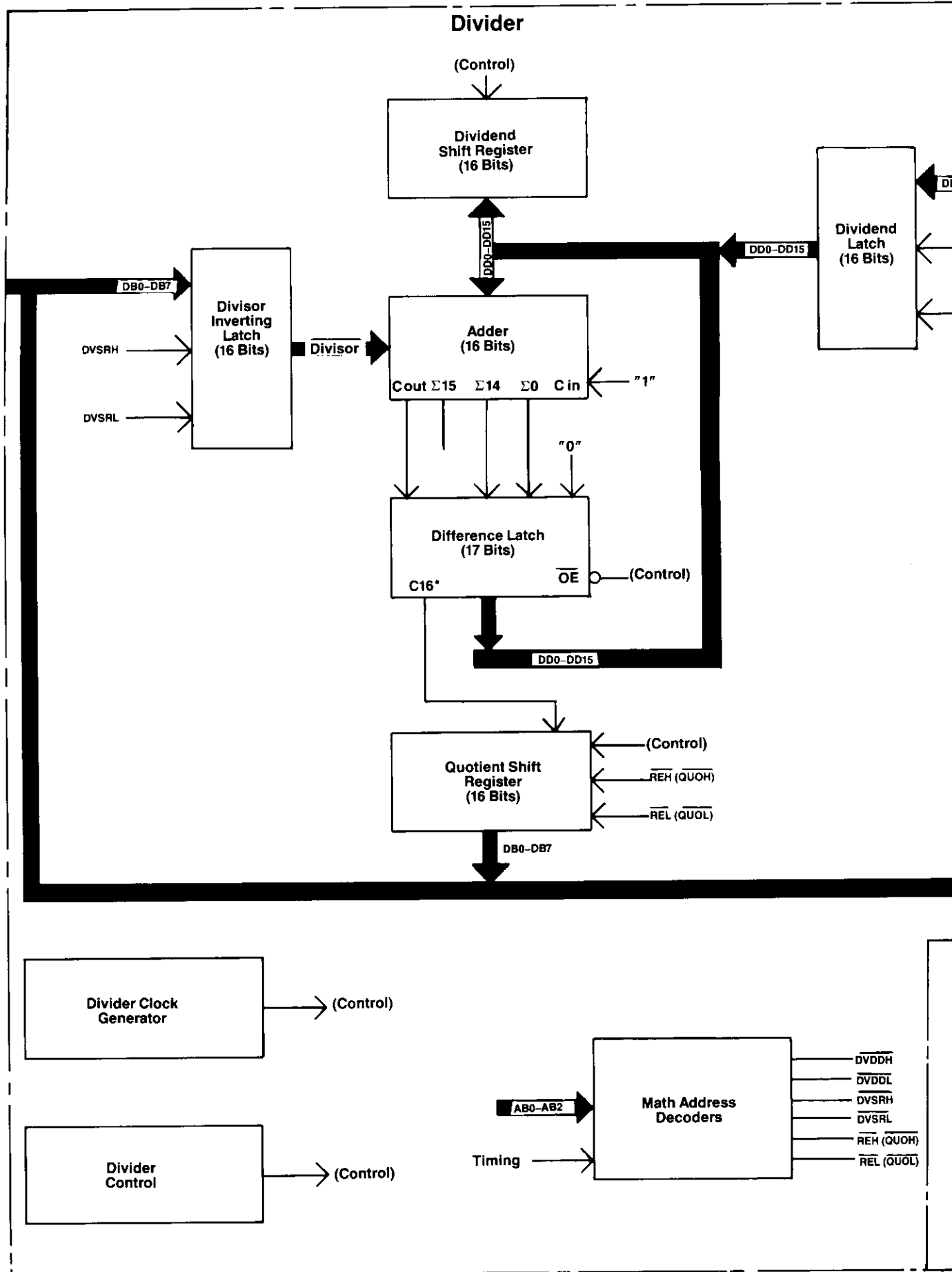
**STAR WARS Divider and Matrix Processor
Detailed Block Diagrams**



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READ/ WRITE	DATA BUS SIGNAL LINES D7 D6 D5 D4 D3 D2 D1 D0								FUNCTION
R/W	D	D	D	D	D	D	D	D	VRAM0
R/W	D	D	D	D	D	D	D	D	VRAM1
R/W	D	D	D	D	D	D	D	D	VRAM2
R/W	D	D	D	D	D	D	D	D	VRAM3
R/W	D	D	D	D	D	D	D	D	VRAM4
R/W	D	D	D	D	D	D	D	D	VRAM5
R	D	D	D	D	D	D	D	D	VROM
R	D								LEFT F/S
R		D							RIGHT F/S
R			D						SPARE 1
R				D					SELF-TEST
R					D				SLAM
R						D			COIN AUX
R							D		COIN L
R								D	COIN R
R	D								MATH RUN
R		D							VGHALT
R			D						LEFT THUMB
R				D					RIGHT THUMB
R					D				SPARE 2
R						D			DIAGN
R							D		Unused
R								D	Unused
R	D	D	D	D	D	D	D	D	OPT 0
R	D	D	D	D	D	D	D	D	OPT 1
R	D	D	D	D	D	D	D	D	ADC
R	D	D	D	D	D	D	D	D	MAINREAD
W	D	D	D	D	D	D	D	D	MAINWR
R	D								MAIN READY FLAG
R		D							SOUND READY FLAG
R/W					D	D	D	D	NOVRAM

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STAR WARS Memory Map -part 1



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HEXA- DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES															
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0000-07FF	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A
0800-0FFF	0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A
1000-17FF	0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	A
1800-1FFF	0	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A
2000-27FF	0	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A
2800-2FFF	0	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A
3000-3FFF	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A
4300	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
	0	1	0	0	0	0	1	1	0	0	0					
4320	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
	0	1	0	0	0	0	1	1	0	0	1					
4340	0	1	0	0	0	0	1	1	0	1	0					
4360	0	1	0	0	0	0	1	1	0	1	1					
4380	0	1	0	0	0	0	1	1	1	0	0					
4400	0	1	0	0	0	1	0	0								0
	0	1	0	0	0	1	0	0								0
4401	0	1	0	0	0	1	0	0								1
	0	1	0	0	0	1	0	0								1
4500-45FF	0	1	0	0	0	1	0	1	A	A	A	A	A	A	A	A

READ/ WRITE	DATA BUS SIGNAL LINES D7 D6 D5 D4 D3 D2 D1 D0								FUNCTION
W									$\overline{\text{EVGGO}}$
W									$\overline{\text{EVGRES}}$
W									$\overline{\text{WDCLR}}$
W									$\overline{\text{IRQCLR}}$
W	D								$\overline{\text{COIN CNTR 2}}$
W	D								$\overline{\text{COIN CNTR 1}}$
W	D								$\overline{\text{LED 3}}$
W	D								$\overline{\text{LED 2}}$
W	D								SASS
W	D								$\overline{\text{PRNGCLR}}$
W	D								$\overline{\text{LED 1}}$
W	D								$\overline{\text{RECALL}}$
W									$\overline{\text{NSTORE}}$
W									$\overline{\text{ADCSTART 0}}$
W									$\overline{\text{ADCSTART 1}}$
W									$\overline{\text{ADCSTART 2}}$
W									$\overline{\text{SOUNDRST}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{REH}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{MW0}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{REL}}$
W								D	$\overline{\text{MW1}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{MW2}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{PRNG}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVSRLH}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVSRL}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVDDH}}$
W	D	D	D	D	D	D	D	D	$\overline{\text{DVDDL}}$
R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM}}$
R/W	D	D	D	D	D	D	D	D	$\overline{\text{MBRAM}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 0}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 1}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 2}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 3}}$
R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 4}}$

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STAR WARS Memory Map -part 2



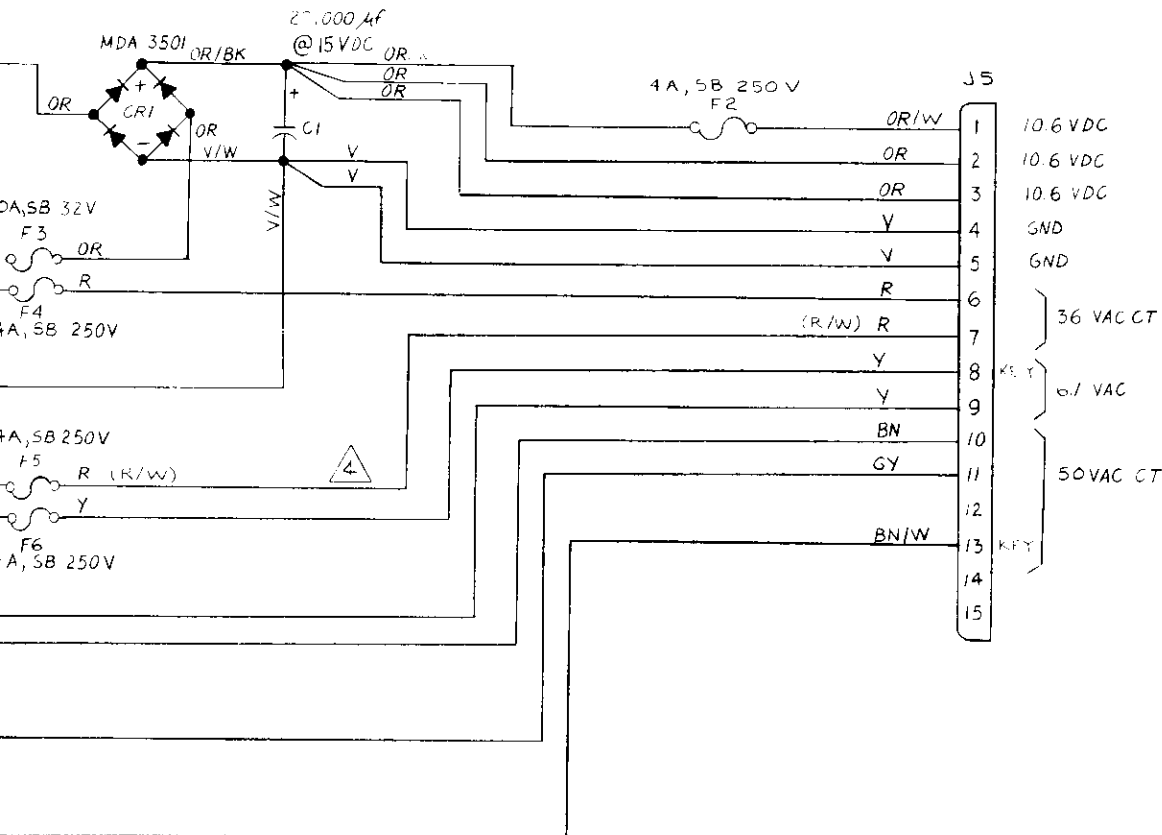
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HEXA- DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES															
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4600	0	1	0	0	0	1	1	0	0	0	0					
4620	0	1	0	0	0	1	1	0	0	0	1					
4640	0	1	0	0	0	1	1	0	0	1	0					
4660	0	1	0	0	0	1	1	0	0	1	1					
4680	0	1	0	0	0	1	1	0	1	0	0			0	0	0
4681	0	1	0	0	0	1	1	0	1	0	0			0	0	1
4682	0	1	0	0	0	1	1	0	1	0	0			0	1	0
4683	0	1	0	0	0	1	1	0	1	0	0			0	1	1
4684	0	1	0	0	0	1	1	0	1	0	0			1	0	0
4685	0	1	0	0	0	1	1	0	1	0	0			1	0	1
4686	0	1	0	0	0	1	1	0	1	0	0			1	1	0
4687	0	1	0	0	0	1	1	0	1	0	0			1	1	1
46A0	0	1	0	0	0	1	1	0	1	0	1					
46C0	0	1	0	0	0	1	1	0	1	1	0				0	0
46C1	0	1	0	0	0	1	1	0	1	1	0				0	1
46C2	0	1	0	0	0	1	1	0	1	1	0				1	0
46E0	0	1	0	0	0	1	1	0	1	1	1					
4700	0	1	0	0	0	1	1	1						0	0	0
	0	1	0	0	0	1	1	1						0	0	0
4701	0	1	0	0	0	1	1	1						0	0	1
	0	1	0	0	0	1	1	1						0	0	1
4702	0	1	0	0	0	1	1	1						0	1	0
4703	0	1	0	0	0	1	1	1						0	1	1
4704	0	1	0	0	0	1	1	1						1	0	0
4705	0	1	0	0	0	1	1	1						1	0	1
4706	0	1	0	0	0	1	1	1						1	1	0
4707	0	1	0	0	0	1	1	1						1	1	1
4800-4FFF	0	1	0	0	1	A	A	A	A	A	A	A	A	A	A	A
5000-5FFF	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A
6000-7FFF	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A
8000-9FFF	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A
A000-BFFF	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A
C000-DFFF	1	1	0	A	A	A	A	A	A	A	A	A	A	A	A	A
E000-FFFF	1	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A

Color X-Y Power Supply Wiring Diagram



NOTES.

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND), & ONE WHITE WIRE (NEUTRAL).
2. USE 4 AMP 5B 250V FUSE AT F1 WITH 220 V & 240 V (EUROPEAN ONLY).
3. CONNECTOR J4B USED IN -04 THRU -06 VERSIONS OF A037396-XX ONLY.
4. ALTERNATE WIRE COLOR IS IN PARENTHESES.

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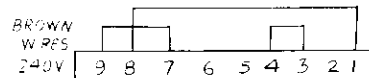
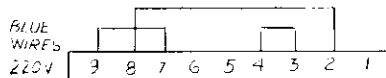
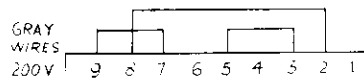
STAR WARS Color X-Y Power Supply Wiring Diagram



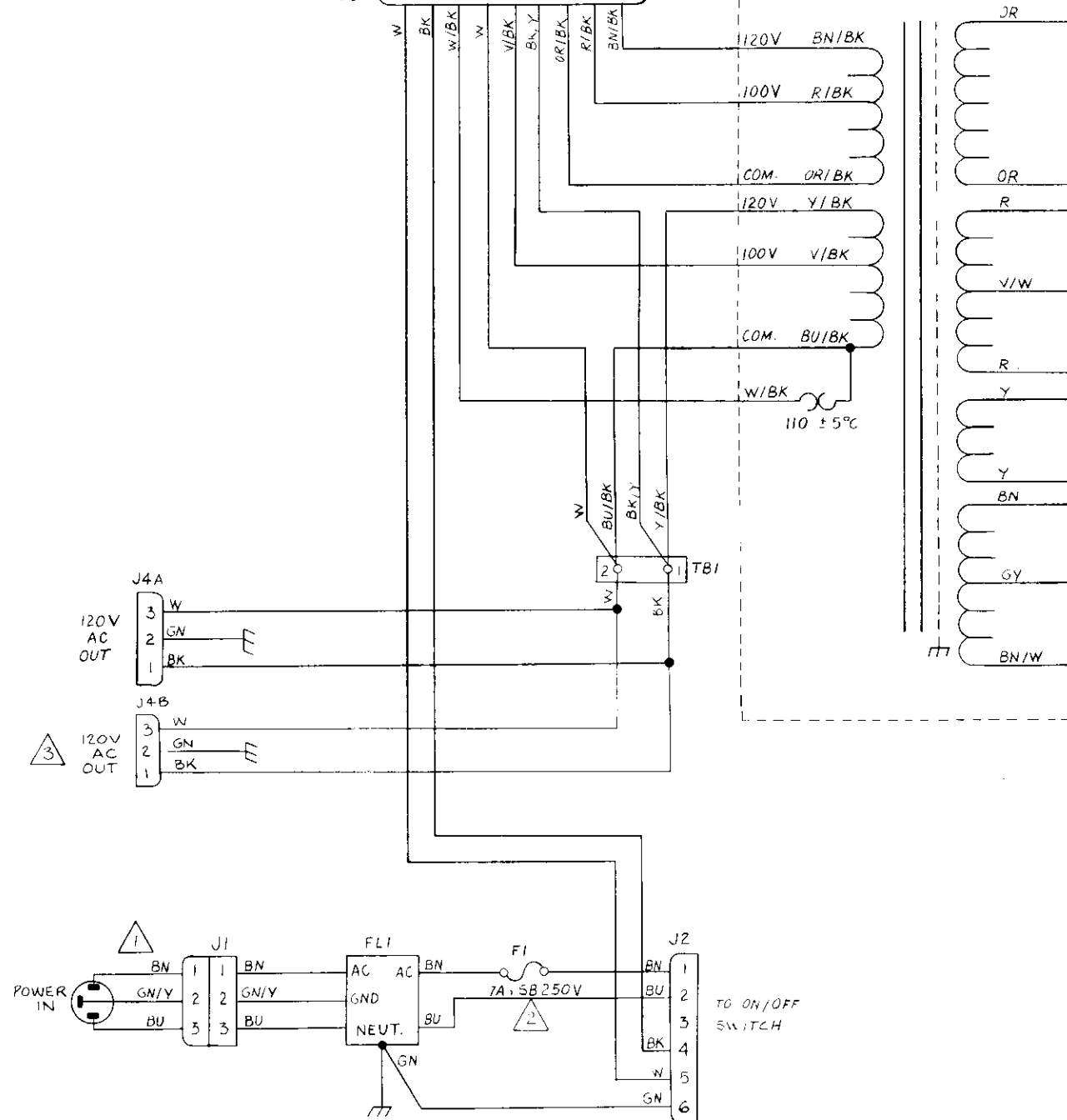
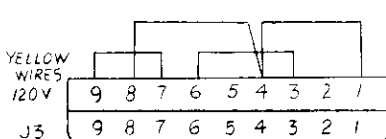
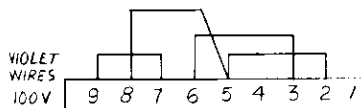
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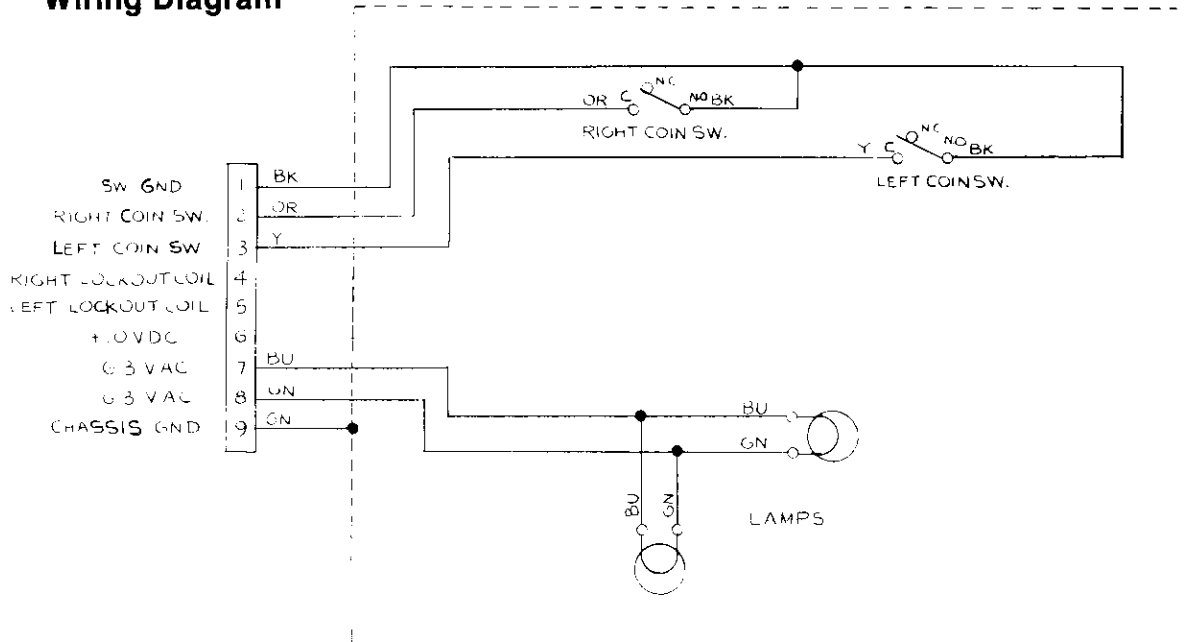
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VOLTAGE SELECTION BLOCKS



Coin Door Wiring Diagram



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STAR WARS Game Interfaces

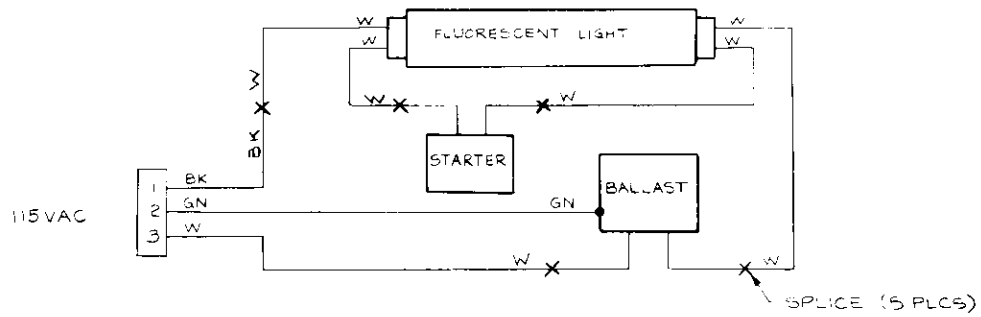


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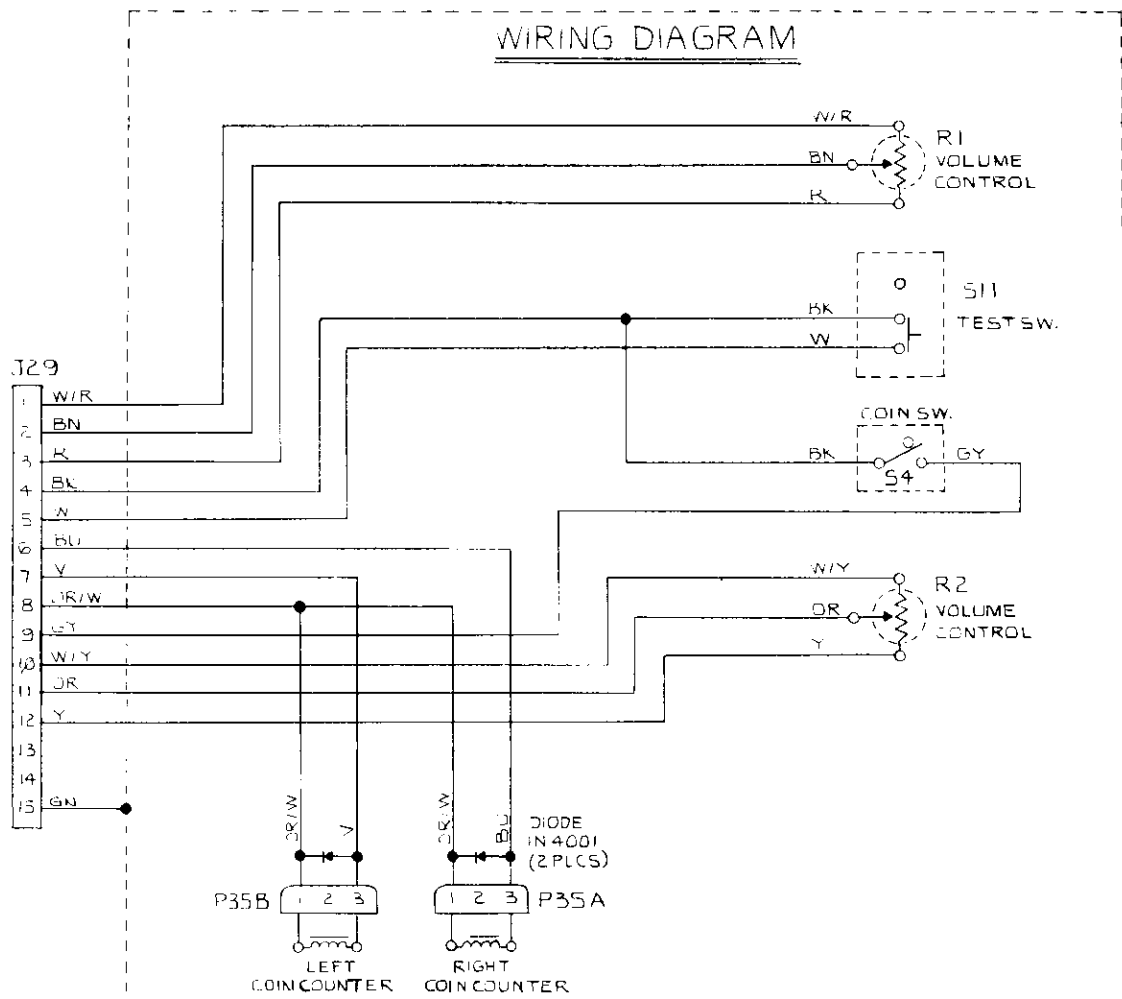
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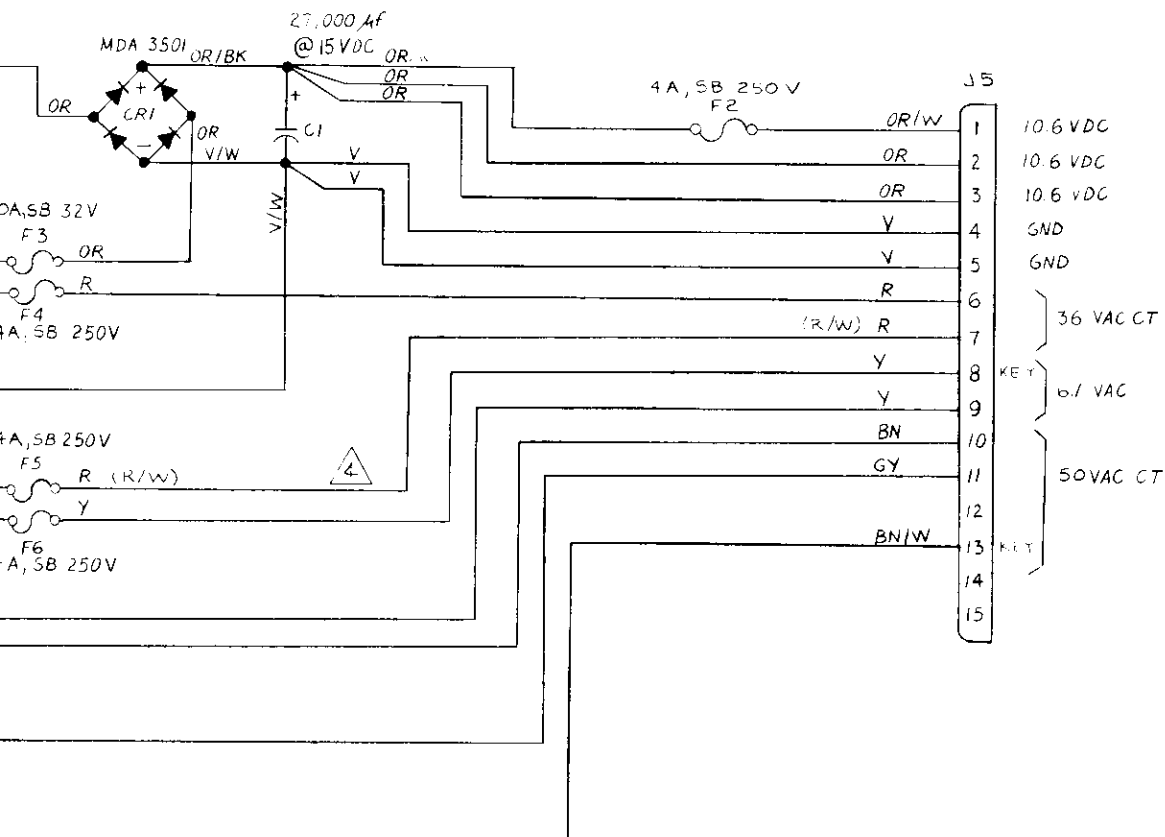
Fluorescent Light Wiring Diagram



Utility Panel Wiring Diagram



Color X-Y Power Supply Wiring Diagram



NOTES:

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2. USE 4 AMP SB 250V FUSE AT F1 WITH 220 V & 240 V (EUROPEAN ONLY).
3. CONNECTOR J48 USED IN -04 THRU -06 VERSIONS OF A037396-XX ONLY.
4. ALTERNATE WIRE COLOR IS IN PARENTHESES.

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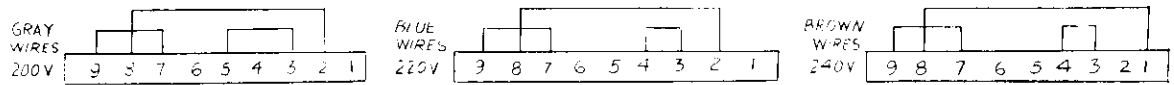
STAR WARS Color X-Y Power Supply Wiring Diagram



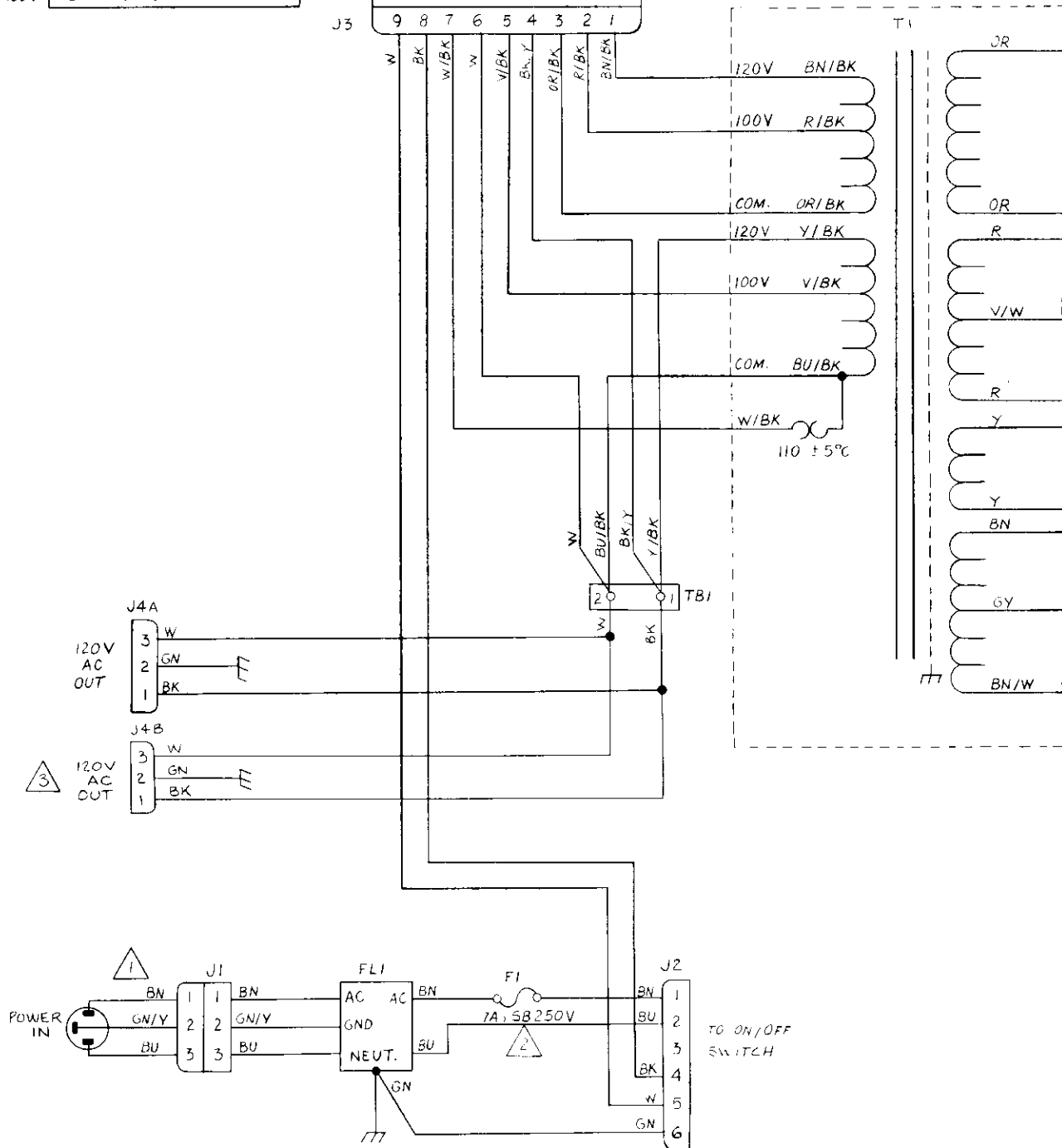
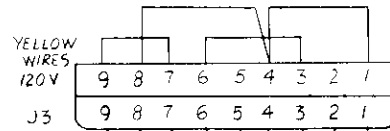
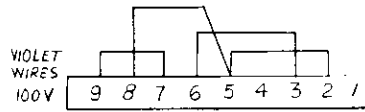
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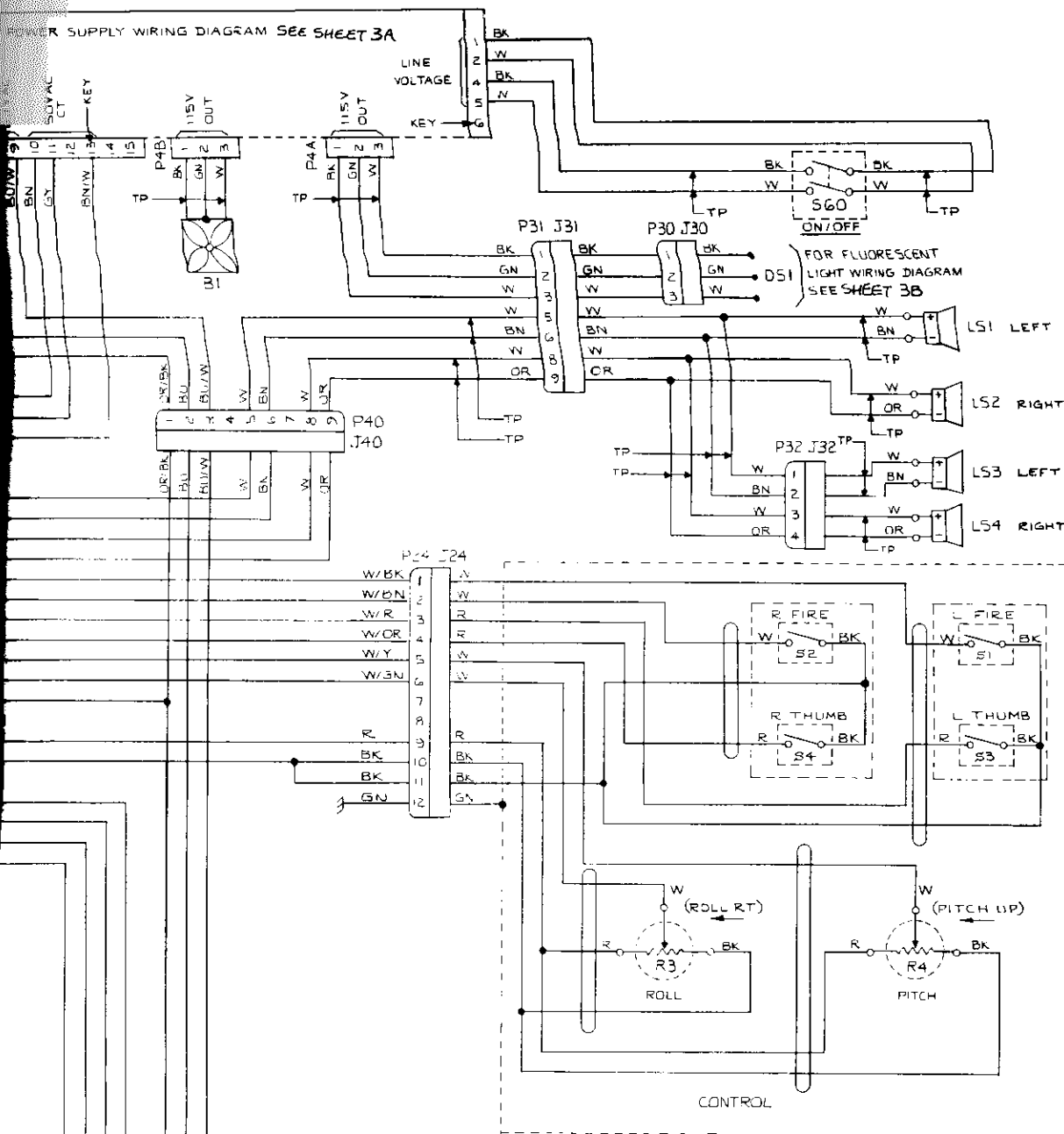
SP-225 Sheet 3A
1st printing



VOLTAGE SELECTION BLOCKS



POWER SUPPLY WIRING DIAGRAM SEE SHEET 3A



FOR CONT. WIRING DIAGRAM SEE SHEET 3B

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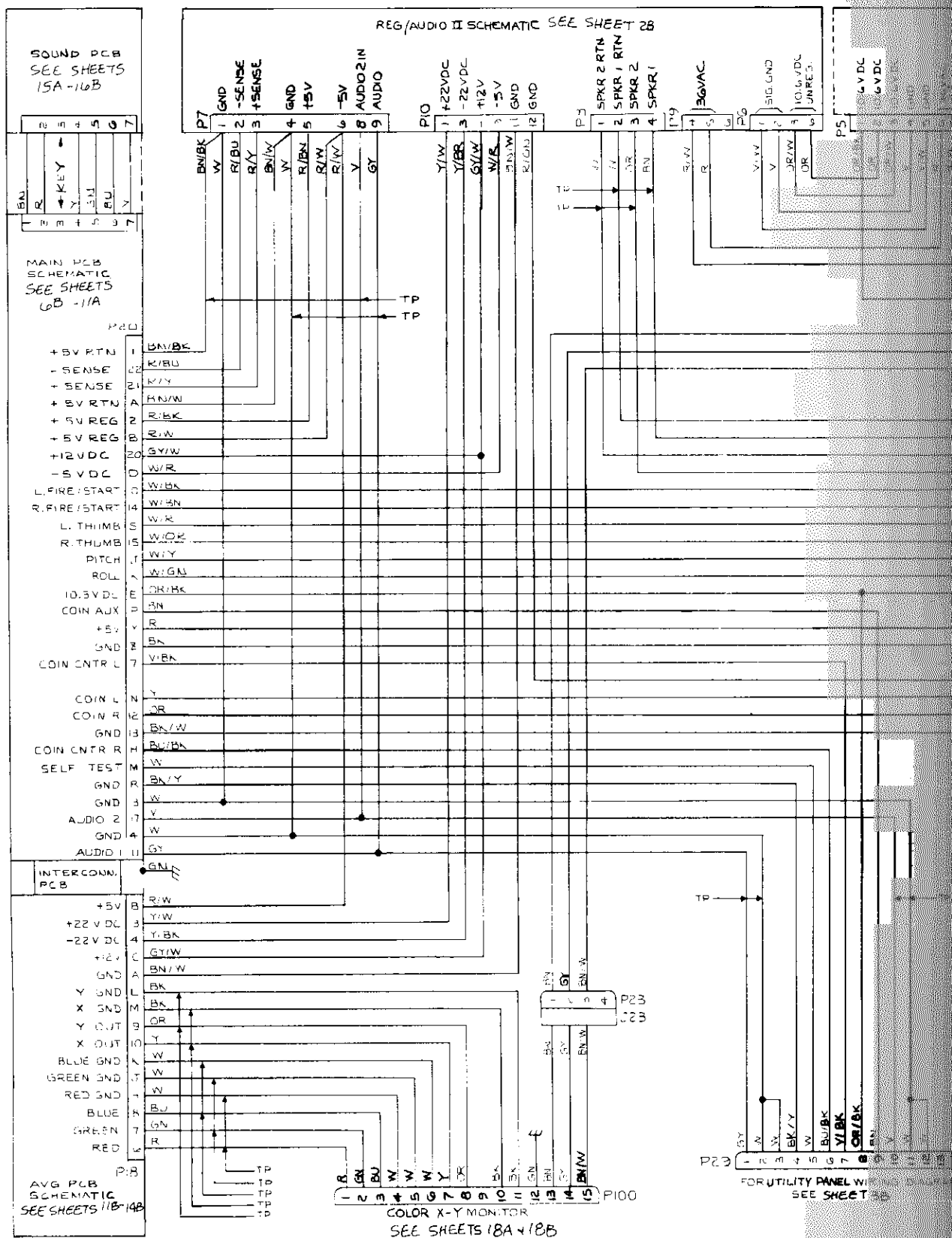
STAR WARS Cockpit Main Wiring Diagram



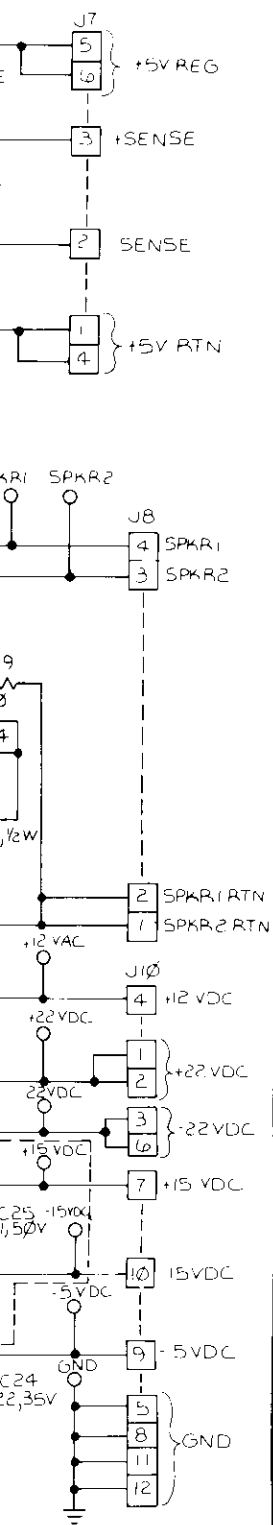
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Star Wars Regulator/Audio II PCB Schematic Diagram



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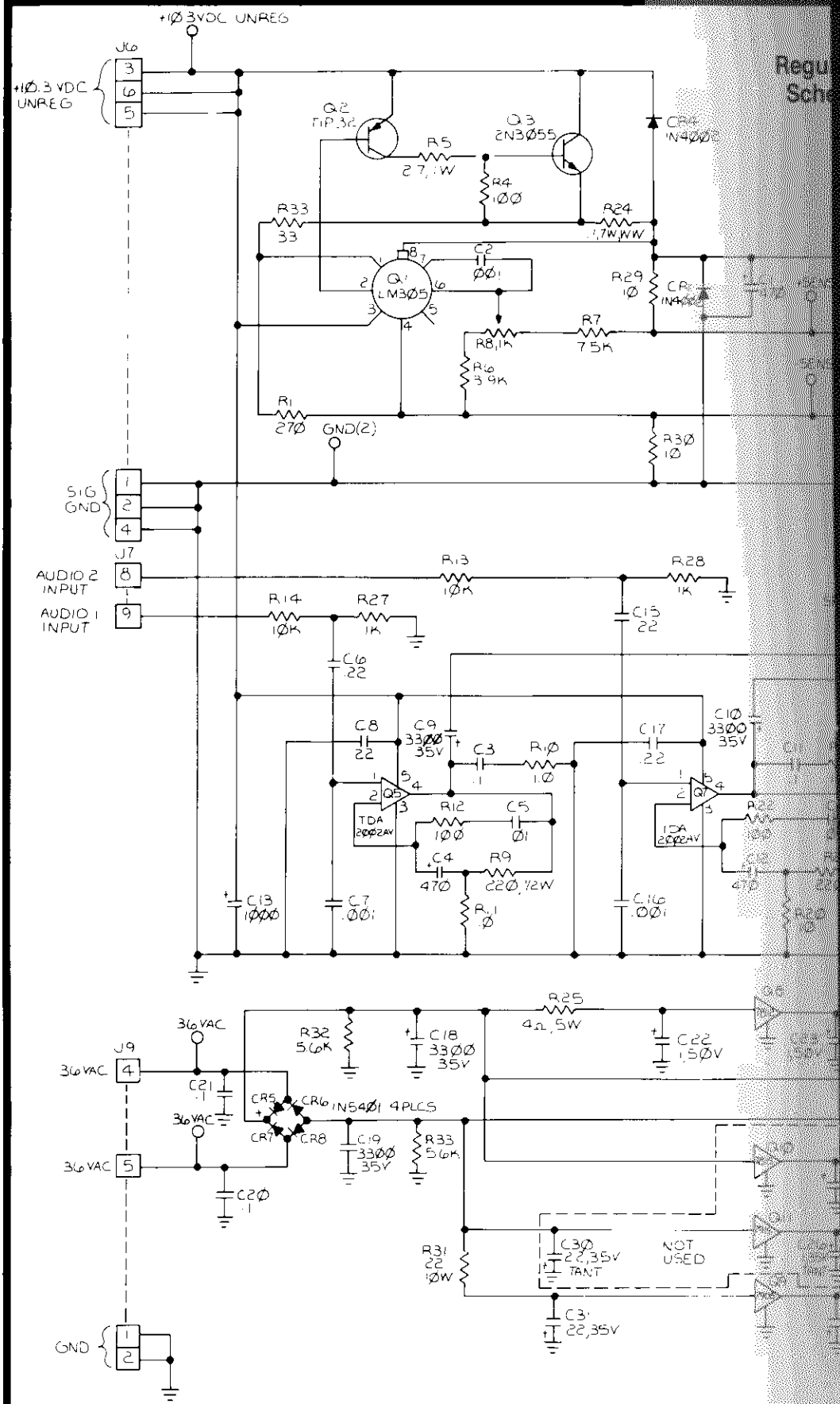
STAR WARS Regulator/Audio II PCB

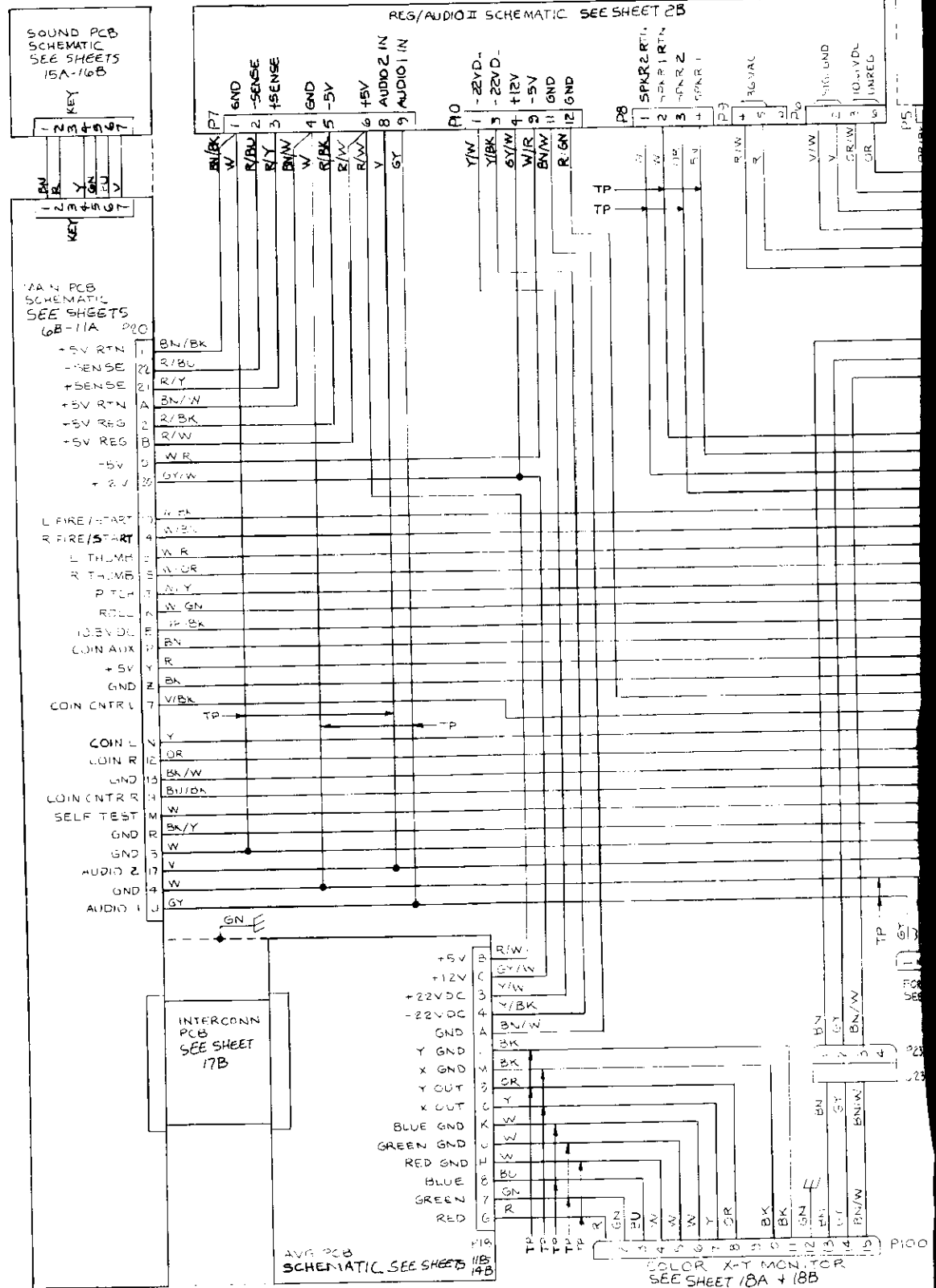


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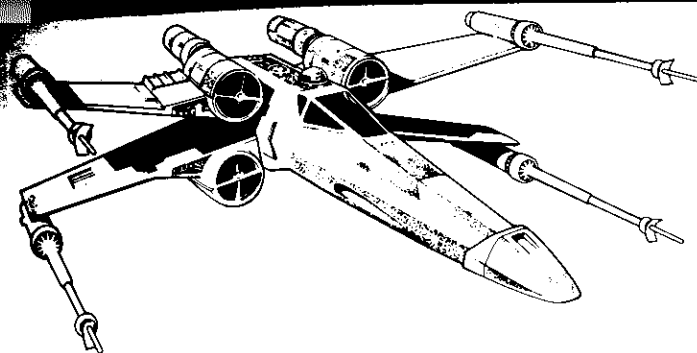


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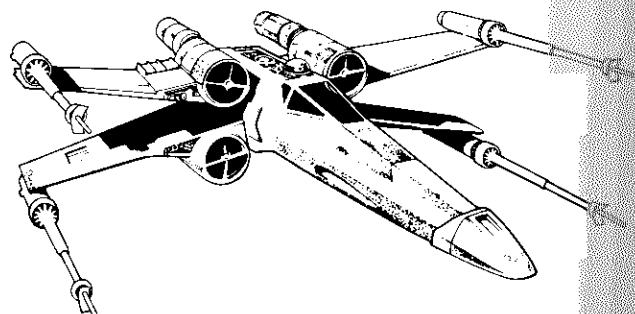
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